



IAC-RK3588-KIT Hardware Manual

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1. Information updates

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3.How to get information

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Version Record

Version No.	Hardware Platform	Description	Date
1.0	IAC-RK3588-MB V1.00	Initial version, first launch	2024-04



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ATTN: This manual introduces the hardware interface of the IAC-RK3588-Kit Development Kit.

I.Preface

1.1.Company Profile

Zhejiang Qiyang Intelligent Technology Co., Ltd., established in 2007, which locates in Hangzhou, Zhejiang, PRC. It is a high-end technological enterprise that specializes in exploitation, fabrication, and selling embedded computer mainboards . With 10 years of experiences, Qiyang has established the completed service chain from the design concept to mass production successfully.

The R&D team is organized by 30 more technical engineers. Qiyang focus on providing functional embedded hardware, software tool and customization solutions. It has been applied to Industrial Control, Internet of Things, New Retail, Smart Medical, Electricity Device, Environmental Surveillance, Charging Pile etc.

With the growth of the business, Qiyang has set up an SMT factory in Zhuji, Zhejiang province, which is 5000 m², with a 2xSMT production line. The SMT factory performs the ISO9001 Quality Management System strictly. Relying on the solid production ability, the SMT factory's annual capacity is about a million sets, which totally guarantee the delivery date.

Qiyang has a thorough sales marketing network, professional sales ,and after-sales team to provide full technical support and service. The business has spread over 120 countries and areas, it helps the clients to introduce the products into the market efficiently and successfully.The combination and extension of research and development, production capacity, and market, that provide a solid foundation for Qiyang to provide specialized, globalized embedded hardware and software.

We offer:

1.Software/Hardware Mainboard

Based on the CPU solution from NXP,Rockchip,MTK,Renesas,TI,Atmel,Cirrus Logic etc, Qiyang provides the ARM development kit/system on module/industrial board and periphery products, paired tools and software for the user do further exploitation.

2.Customization Service

Fully taking the advantage of the technical accumulation on the ARM platform and Linux, Android, Ubuntu OS, Qiyang provides the efficient OEM/ODM service to the users.

Sincerely thanks for using Qiyang's product, we will try our best to offer you the technical supports!

1.2. IAC-RK3588-KIT Development Board Use Suggestion:

1. Please read the instructions before using the IAC-RK3588-Kit development Kit;
2. Before using, please check the packing list and see whether there is a missing file in the folder;

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Website: <http://www.qiytech.com>

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3. Please understand the basic structure and composition of IAC-RK3588-CM SOM, including the hardware resource allocation, and expansion pin definition, etc.;
4. If you want to develop based on Debian Linux or Android OS, to flash the program on the development board, we suggest you to read another article ***IAC-RK3588-Kit User Manual***.
5. IAC-RK3588-CM SOM module accept batch orders.

II. Introduction

2.1. Overview

RK3588 is a low power, high performance processor for ARM-based PC and Edge Computing device, personal mobile internet device and other digital multimedia applications, and integrates quad-core Cortex-A76 and quad-core Cortex-A55 with separately NEON coprocessor.

Many embedded powerful hardware engines provide optimized performance for high-end application. RK3588 supports H.265 and VP decoder by 8K@60fps, H.264 decoder by 8K@30fps, and AV1 decoder by 4K@60fps, also support H.264 and H.265 encoder by

8K@30fps, high-quality JPEG encoder/decoder, specialized image preprocessor and postprocessor.

Embedded 3D GPU makes RK3588 completely compatible with OpenGL ES 1.1, 2.0, and 3.2, OpenCL up to 2.2 and Vulkan 1.2. Special 2D hardware engine with MMU will maximize display performance and provide very smoothly operation.

RK3588 introduces a new generation totally hardware-based maximum 48-Megapixel ISP (image signal processor). It implements a lot of algorithm accelerators, such as HDR, 3A, LSC, 3DNR, 2DNR, sharpening, dehaze, fisheye correction, gamma correction and so on.

The build-in NPU supports INT4/INT8/INT16/FP16 hybrid operation and computing power is up to 6TOPs. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted.

RK3588 has high-performance quad channel external memory interface (LPDDR4/LPDDR4X/LPDDR5) capable of sustaining demanding memory bandwidths, also provides a complete set of peripheral interface to support very flexible applications.

RK3588 Processor Block Diagram:

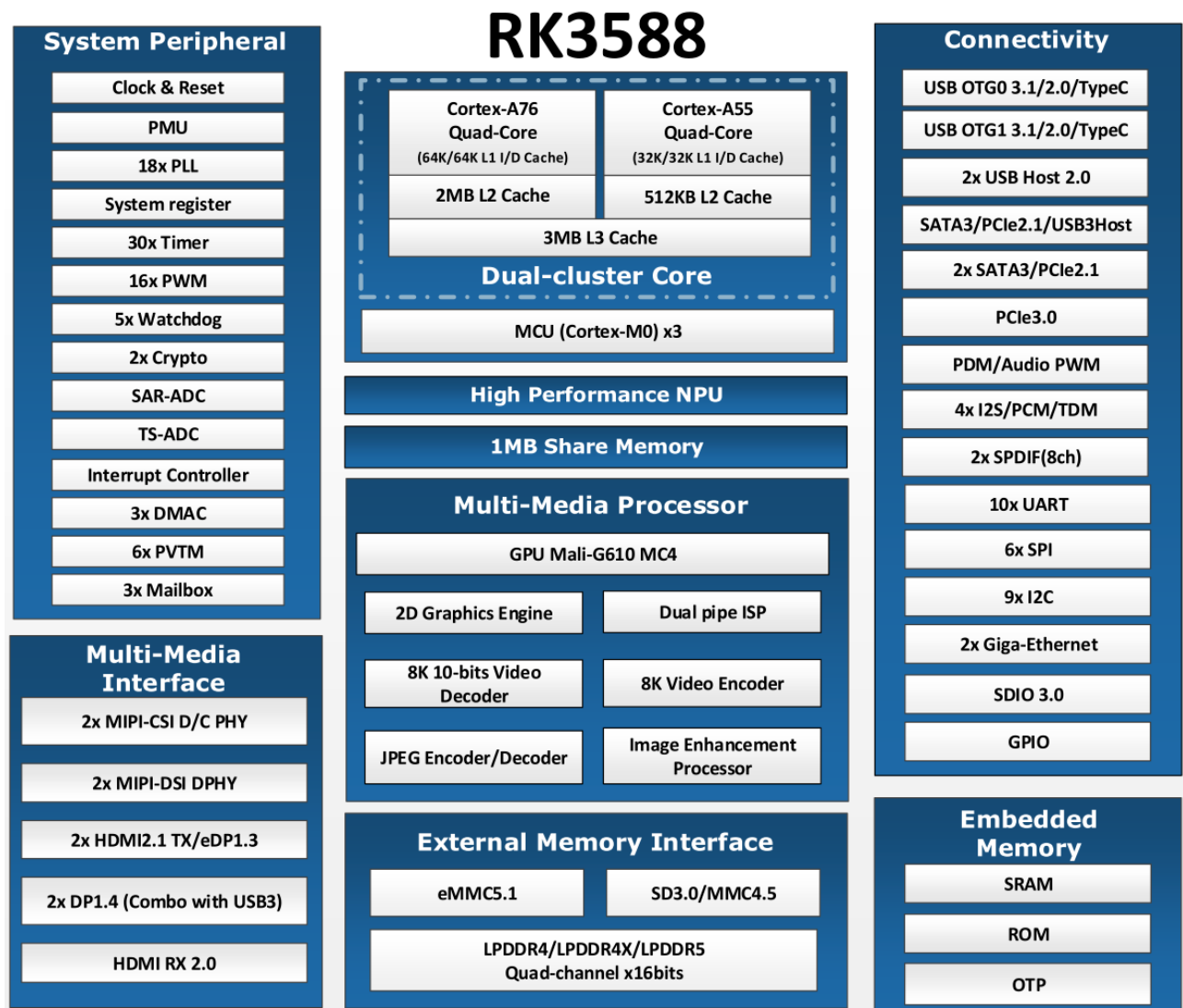


Figure 1

Detailed parameters:

CORE	CPU	● A Quad-core Cortex-A76 and a Quad-core Cortex-A55, the CPU frequency reaches up to 2.4Ghz and 1.8Ghz ● Integrated 64KB L1 instruction cache, 64KB L1 data cache and 512KB L2 cache for each Cortex-A76 ● Integrated 32KB L1 instruction cache, 32KB L1 data cache Display and 128KB L2 cache for each Cortex-A55 ● Big cluster Quad-core Cortex-A76 and little cluster Quad-core Cortex-A55 share 3MB L3 cache ● Support ARM-V8 architecture.
	MCU	● Three Cortex-M0 MCUs inside RK3588 ● MCU in VD_PMU integrate 16KB Cache and 16KB TCM ● MCU in VD_NPU integrate 16KB Cache and 64KB TCM ● MCU in PD_CENTER integrate 32KB TCM ● Integrated Programmable Interrupt Controller, all IRQ lines connected to GIC ● for CPU also connect to MCU in VD_PMU(PMU_M0) and PD_CENTER(DDR_M0) ● Integrated Debug Controller with JTAG interface
Memory	Internal on-chip memory	● Support system boot from the following device: ➢ SPI interface ➢ eMMC interface ➢ SD/MMC interface ● Support system code download by the following interface: ➢ USB OTG interface ● Share Memory in the voltage domain of VD_LOGIC ● PMU SRAM in VD_PMU for low power application
	External off-chip memory	● Dynamic Memory Interface ◆ Compatible with JEDEC standards LPDDR4/LPDDR4X/LPDDR5 ◆ Support four channels, each channel 16bits data widths ◆ Support up to 2 ranks (chip selects) for each channel ◆ Totally up to 32GB address space ◆ Low power modes, such as power-down and self-refresh for SDRAM ● eMMC Interface ◆ Fully compliant with JEDEC eMMC 5.1 and eMMC 5.0 specification ◆ Backward compliant with eMMC 4.51 and earlier versions specification. ◆ Support HS400, HS200, DDR50 and legacy operating modes ◆ Support three data bus width: 1bit, 4bits or 8bits ● SD/MMC Interface ◆ Compatible with SD3.0, MMC ver4.51

		◆ Data bus width is 4bits ● Flexible Serial Flash Interface(FSPI) ◆ Support transfer data from/to serial flash device ◆ Support 1bit, 2bits or 4bits data bus width ◆ Support 2 chips select
CPU	GPU	● ARM Mali-G610 MP4 ● Support high performance OpenGL ES 1.1,2.0, OpenCL 2.2, Vulkan1.2, etc. ● Embedded 4 shader editor core and shared layered shader. ● Provide MMU with 4x256KB and L2 cache. ● Newest Valhall architecture; ARM frame buffer compression (AFBC) 1.3. ● Support embedded single chip serial cable debugging.
	NPU	● .Neural network acceleration engine with processing performance up to 6 TOPS ● Include triple NPU core, and support triple core co-work, dual core co-work, and work independently ● Support integer 4, integer 8, integer 16, float 16, Bfloat 16 and tf32 operation ● Embedded 384KBx3 internal buffer, multi-task, multi-scenario in parallel ● Support deep learning frameworks: TensorFlow, Caffe, Tflite, Pytorch, Onnx NN,
	ISP	● Maximum input ■ 48M: 8064x6048@15 dual ISP ■ 32M: 6528x4898@30 dual ISP ■ 16M: 4672x3504@30 single ISP ● Support multi-sensor ISP
	VICAP	● Support BT601, BT656, BT1120 ● Support receiving six interfaces of MIPI CSI/DSI, up to four IDs for each interface ● Support five CSI data formats: RAW8/10/12/14, YUV422 ● Support three modes of HDR: virtual channel mode, identification code mode, line counter mode ● Support RAW data through to ISP0/1
	VPU	Video Decoder ● Real-time video decoder of MPEG-1, MPEG-2, MPEG-4, H.263, H.264, H.265, VC-1, VP9, VP8, MVC, AV1 ● MMU Embedded, multi-channel decoder in parallel for less resolution ● H.264 AVC/MVC Main10 L6.0: 8K@30fps (7680x4320) ; ● VP9 Profile0/2 L6.1: 8K@60fps (7680x4320) ; ● H.265 HEVC/MVC Main10 L6.1: 8K@60fps (7680x4320) ; ● AVS2 Profile0/2 L10.2.6: 8K@60fps (7680x4320) ; ● AV1 Main Profile 8/10bit L5.3: 4K@60fps (3840x2160) ;

		● MPEG-2 up to MP: 1080p@60fps (1920x1088) ; ● MPEG-1 up to MP: 1080p@60fps (1920x1088) ; ● VC-1 up to AP level 3: 1080p@60fps (1920x1088) ; ● VP8 version2:1080p@60fps (1920x1088) ; Video Encoder ● Real-time H.265/H.264 video encoding ● Support up to 8K@30fps ● Multi-channel encoder in parallel for less resolution
Video Output	VOP	Video Ports ● Video Port0, max output resolution: 7680x4320@60Hz ● Video Port1, max output resolution: 4096x4320@60Hz ● Video Port2, max output resolution: 4096x4320@60Hz ● Video Port3, max output resolution: 2048x1080@60Hz Cluster 0/1/2/3 ● Max input and output resolution 4096x4320 ● Support AFBCD ● Support RGB/YUV/YUYV format ● Support scale up/down ratio 4~1/4 ● Support rotation ESMART 0/1/2/3 ● Max input and output resolution 4096x4320 ● Support RGB/YUV/YUYV format ● Support scale up/down ratio 8~1/8 ● Support 4 region Overlay ● Support up to 8 layers overlay: 4 cluster/4 esmart ● Support RGB/YUV domain overlay POST process: ● HDR10/HDRHLG ● HDR2SDR/SDR2HDR ● 3D-LUT/P2I/CSC/BCSH/DITHER/CABC/GAMMA/COLORBAR. Write back: ● Format: ARGB8888/RGB888/RGB565/YUV420 ● Max resolution:1920x1080。
Display Interface	HDMI/EDP TX	● Support two HDMI/eDP TX combo interface, but HDMI and eDP can not work at the same time for each interface. ● Support x1, x2 and x4 configuration for each interface ● Support all the data rates for HDMI FRL: 3, 6, 8, 10 and 12Gbps ● Support 1.62Gbps, 2.7Gbps and 5.4Gbps for eDP ● Support up to 7680x4320@60Hz for HDMI TX, and 4K@60Hz for eDP

		- Support RGB/YUV(up to 10bit) format for HDMI TX, EDP support 8/10 bit. - Support RGB, YCbCr 4:4:4, YCbCr 4:2:2 video format.
	DP TX	- Support 2 DP TX 1.4a interface which combo with USB3.1 Gen1 - Support 1/2/4lanes for each interface, Support HDCP2.3, HDCP 1.3 - Support 1.62Gbps, 2.7Gbps, 5.4Gbps and 8.1Gbps Serializer - Support RGB/YUV(up to 10bit) format, Support up to 7680x4320@30Hz - Support Single Stream Transport(SST), support DP Alt mode on USB Type-C
	MIPI DSI	- Support 2 MIPI DPHY 2.0 or CPHY 1.1 interface - Support 4 data lanes and 4.5Gbps maximum data rate per lane for DPHY - Support 3 data trios and 2.0Gsps maximum data rate per trio for CPHY - Support dual MIPI display: left-right mode, support max resolution 4K@60Hz - Support RGB(up to 10bit) format, support DSC 1.1/1.2a
	BT1120	Support RGB(up to 8bit) format, up to 150MHz data rate, support up to 1920x1080@60Hz
Video Input Interface	MIPI	MIPI interface - Two MIPI DC(DPHY/CPHY) combo PHY - Support to use DPHY or CPHY - Each MIPI DPHY V1.2, 4lanes, 2.5Gbps per lane - Each MIPI CPHY V1.1, 3lanes, 2.5Gsps per lane Four MIPI CSI DPHY - Each MIPI DPHY V1.2, 2lanes, 2.5Gbps per lane - Support to combine 2 DPHY together to one 4lanes Support camera input combination: 2 MIPI DCPHY + 4 MIPI CSI DPHY(2 lanes), totally support 6 cameras input 2 MIPI DCPHY + 1 MIPI CSI DPHY(4 lanes) + 2 MIPI CSI DPHY(2 lanes), totally support 5 cameras input 2 MIPI DCPHY + 2 MIPI CSI DPHY(4 lanes), totally support 4 cameras input
	DVP	- One 8/10/12/16-bit standard DVP interface, up to 150MHz input data - Support BT.601/BT.656 and BT.1120 VI interface - Support the polarity of pixel_clk, hsync, vsync configurable
	HDMI RX	- Single-port HDMI 2.0 RX PHY, 4 lanes, no sideband channels - Data rate support in HDMI 2.0 mode,6Gbps down to 3.4Gbps - Data rate support in HDMI 1.4 mode,3.4Gbps down to 250Mbps - HDMI 2.0 video formats:TMDS Scrambler to enable support for 2160p@60 Hz with RGB/YCbCr4:4:4 or YCbCr4:2:2 - Supports YCbCr 4:2:0 to enable 2160p@60Hz at lower HDMI link speeds - HDMI 1.4b video formats:All CEA-861-E video formats up to 1080p@120Hz, support 4K x 2K video formats(3840x2160p@24Hz/25Hz/30Hz and 4096x2160p@24Hz)

		● HDMI 1.4b 3D video modes with up to 340 MHz(TMDS clock) ● Support HDCP2.3 and HDCP1.4
Audio Interface	I2S	● I2S0/I2S1 with 8 channels: I2S0 support up to 8 channels TX or 8 channels RX path, I2S1 support up to 8 channels TX and 8 channels RX path, I2S2/I2S3 support up to 2 channels for TX and 2 channels RX path. ● I2S0/I2S support TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer ● Sample rate up to 192KHz, audio resolution from 16bits to 32bits, provides master and slave work mode, software configurable ● Support 3 I2S formats (normal, left-justified, right-justified), support 4 PCM formats (early, late1, late2, late3) ● I2S, PCM and TDM mode cannot be used at the same time on I2S0/I2S1; I2S and PCM cannot be used at the same time on I2S2/I2S3.
	SPDIF	● Support two 16-bit audio data store together in one 32-bit wide location ● Support biphase format stereo audio data output ● Support 16, 20, 24 bits audio data transfer in linear PCM mode, support non-linear PCM transfer
	PDM	● PDM0/1 support up to 8 channels, support PDM master receive mode ● Sample rate up to 192KHz, audio resolution from 16bits to 24bits
	DAC	● Support 2 channels digital DAC, support I2S/PCM interface, master and slave mode ● Support 16 bit sample resolution ● Support three modes of mixing for every digital DAC channel, support volume control
	VAD	● Support read voice data from I2S/PDM, support voice amplitude detection ● Support Multi-Mic array data storing, support a level combined interrupt
Connectivity	SDIO	● Support 4-bit data bus widths, compatible with SDIO3.0 protocol
	ENET	● Support two Ethernet controllers ● Support 10/100/1000-Mbps data transfer rates with the RGMII interfaces ● Support 10/100-Mbps data transfer rates with the RMII interfaces ● Support both full-duplex and half-duplex operation
	USB	● Support USB3.1 Gen1, equal to USB3.2 Gen1 and USB3.0, up to 5Gbps data rate ● Embedded 2 USB3.1 OTG interfaces which combo with DP TX (USB3OTG_0 and USB3OTG_1) ● Embedded 1 USB3.1 Host interface which combo with Combo PIPE PHY2 (USB3OTG_2) ● USB2.0 PHY support Battery Charge detection ● Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode

	Multi PHY	- Support three Combo PIPE PHYs with PCIe2.1/SATA3.0/USB3.1 controller - PCIe2.1: Support 1 lane for each PCIe2.1 interface, 5Gbps data rate, t Root Complex(RC) only, compatible with PCI Express Base Specification Revision 2.1 - SATA3.0*3: Support eSATA, support 1 port for each SATA interface, 6Gbps data rate, compatible with Serial ATA 3.1 and AHCI revision 1.3.1
	PCIe3.0	- Compatible with PCI Express Base Specification Revision 3.0 - Support dual operation mode: Root Complex(RC) and End Point(EP) - Support data rates: 2.5Gbps(PCIe1.1), 5Gbps(PCIe2.1), 8Gps(PCIe3.0) - Support aggregation and bifurcation with 1x 4lanes, 2x 2lanes, 4x 1lanes and 1x 2lanes + 2x 1lanes
	CAN	CAN *3, support CAN2.0 protocol
	SPI	- Support 6 SPI Controllers(SPI0-SPI4) - Support two chip-select output, support serial-master and serial-slave mode, software-configurable
	I2C	- Support 9 I2C Master(I2C0-I2C8) - Support 7bits and 10bits address mode - Software programmable clock frequency - Data on the I2C-bus can be transferred at rates of up to 100k bits/s in the Standard-mode, up to 400k bits/s in the Fast-mode
	UART	- Support 10 UART interfaces(UART0-UART9), embedded two 64-byte FIFO for TX and RX operation respectively - Support 5bit, 6bit, 7bit, 8bit serial data transmit or receive - Standard asynchronous communication bits such as start, stop and parity - Support different input clock for UART operation to get up to 4Mbps baud rate - Support auto flow control mode for all UART - UART2 DEBUG

2.2. Development Board Resources

Resource	CPU	RockChip RK3588
	Process or	Quad ARM® Cortex™-A55 Core+ Quad ARM® Cortex™-A76 Core, up to 2.4Ghz. 3*ARM® Cortex™-M0 MCU
	GPU	Mali-G610 MP4 Support OpenGL ES 1.1/2.0/3.2, OpenCL 2.2, Vulkan 1.2
	VPU	Support 8K 30fps H.264 video decoder Support 8K 60fps H.265/VP9/AVS2 video decoder

		Support 4K 60fps AV1 video decoder Support 1080P 60fps MPEG-2/MPEG-1/VC-1/VP8 video decoder Support up to 8K 30fps H.265/H.264 video decoder
	ISP	48M in max.
	NPU	Neural Process Unit: 6TOPS
	RAM	8GB LPDDR4 (16GB in max.)
	Flash	64GB eMMC (128GB optional)
	PMIC	Rockchip RK806 PMU
	Ethernet	2-ch network chipset adopts RGMII mode to support 10M/100M/1000Mbps.
	Connectivity	1*UART To USB DEBUG port
		2*RS232 port (3-wire RS232 port)
		1-ch RS485 port
	Display	2* 4 channel MIPI_DSI port, up to 4K@60Hz .
		1*HDMI port (HDMI2.1), up to 7680x4320p@60Hz
		1*eDP port, up to 4K@60Hz
	Audio	Line out, speaker
		Line out, stereo, headphone socket
		Single channel MIC audio input
	USB	4*USB2.0 Type-A HOST
		1*USB3.0 OTG Type-c
		1*USB3.0 OT&DP Type-c
	Camera	4*MIPI-CSI (4-channel), support 4*camera input simultaneously, up to 4*2k@120Hz
	Input	Standard I2C capacitive touch port 1*HDMI RX port, up to 2160p@60Hz
	Expansion#1	M.2 B-KEY, to connect 4G/5G module M.2 E-KEY, to connect WIFI module M.2 M-KEY, to connect SSD module
	Expansion #2	15*GPIO (3.3V)
	Storage	1*TF card socket

	Others	Reset Circuit ,Watchdog, RTC
	Power Input	+12V
SDK	Development Tools	Environment: Virtual Machine VM15.5.0+Ubuntu20.04 or other Linux environment.
		Application developing and debugging tool
		Cross compiler
		Common terminal developing and debugging tool
	System Image	Image file which the OS relates to
	Test Program	Demo test program and test source code
	Source Code	Bootloader, Kernel, file system source code
	Manual	Hardware Manual, Test Manual, Device Manual, etc.
	Schematic	Schematic of interface board (PDF format)
	Mechanical Drawing	Size & Structure of the interface board (DXF format)
Electricity	Layer/Size	SOM Size:68mm*55mm,10-layer high precision immersion gold technology
		Carrier Board Size: 220mm*140mm,6-layer high precision immersion gold technology
	Power Consumption	To be continued
	Working Temperature	0℃ ~ +70℃ (-40℃ ~ +85℃ optional)
	Storage Temperature	-0℃ ~ +70℃
	Humidity	10%~90%,non-condensation
	Options	Standard option::8GB DDR/64GB eMMC

2.3.SOM Module Resource

IAC-RK3588-CM SOM module adopts 10-layer PCB high precision immersion gold process, high TG board, with reliable electricity and anti-interference performance. Integrated with CPU,LPDDR4,eMMC, PMU, etc. It adopts board to board receptacle which the pin-out is up to 400 pins. It fully extended RK3568 processor resources, and it is available to design a customization carrier board based on the multiplexed pins.

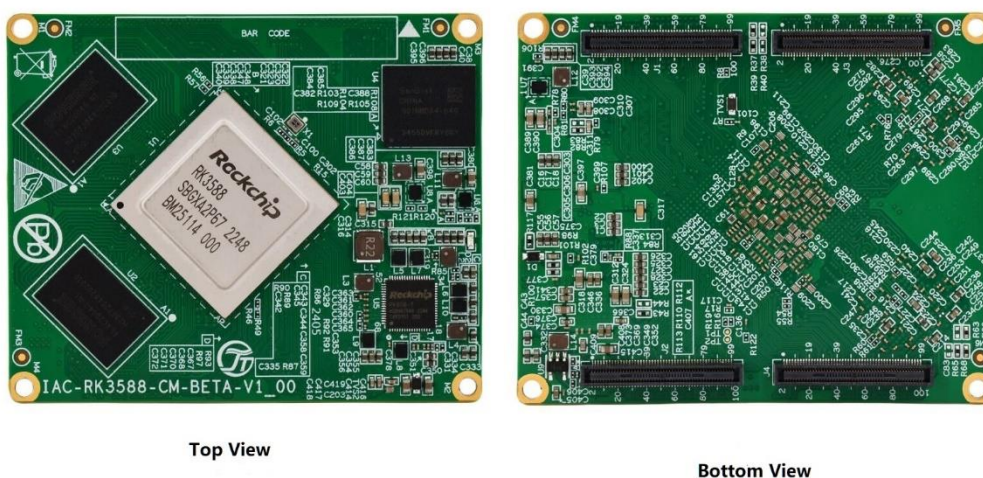


Figure 2

- ◆ Onboard with RockChip RK3568 processor;
- ◆ Onboard with 8GB LPDDR4, 64GB eMMC (Standard option);
- ◆ The SOM adopts 10-layer PCB high precision immersion gold process;
- ◆ SOM size: 68mm*55mm, it suits for various application scenarios;
- ◆ The SOM adopts 4 pieces of 2*50Pin board to board receptacle to extract signals of SOM;
- ◆ +4V DC, onboard with PMU;
- ◆ Support Debian 11.0
- ◆ Support Android 13.0

To know the pin definition which is extract from the SOM module, please check the below sector of Connectors on Carrier Board;

III. Connectors on Carrier Board

Block Diagram- Top View

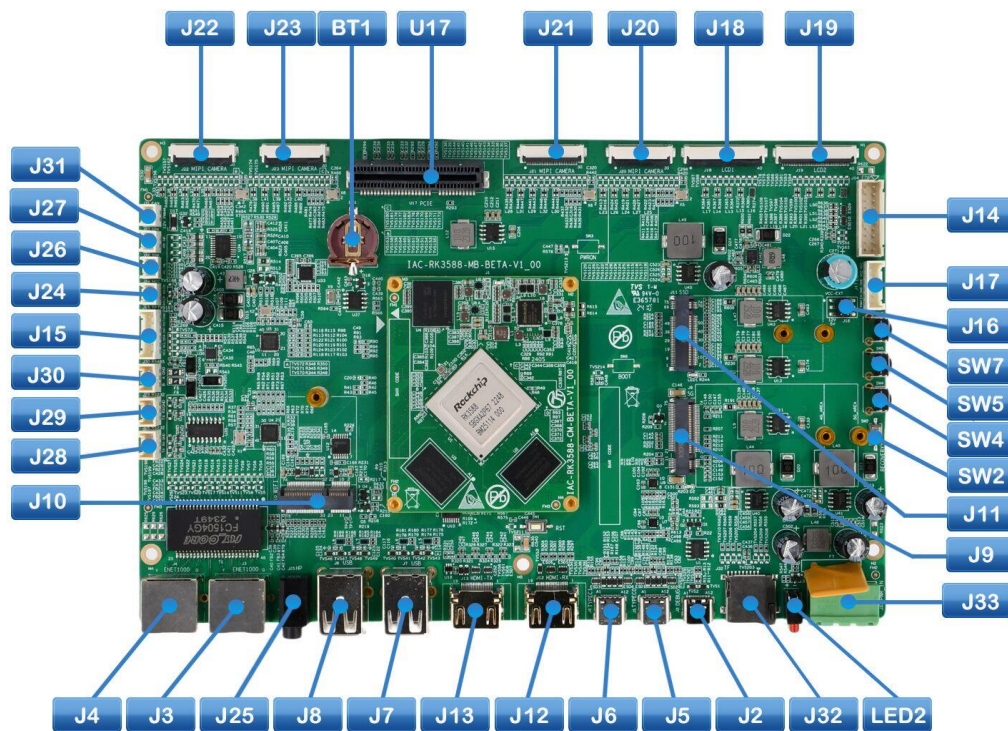


Figure 3



Block Diagram- Bottom View

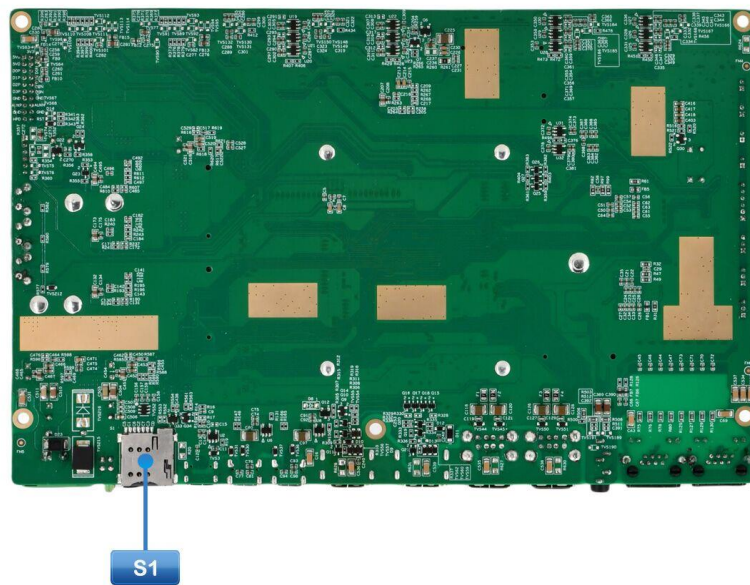


Figure 4

3.1. Basic functions

Label	Functions
J33	DC12V
LED2	Power indicator, system running indicator
J32	TF socket
J2	USB DEBUG port
J5	Type-c OTG
J6	Type-c USB3.0&DP
J12	HDMI RX
J13	HDMI Output
J7	USB2.0 HOST
J8	USB2.0 HOST
J25	3.5mm Headphone socket
J3	Gigabit Ethernet Port
J4	Gigabit Ethernet Port
J10	M.2 E-KEY (PCI-E2.0) port
J28	RS232
J29	RS232
J30	RS485
J15	I2C touch panel port
J24	MIC
J26	Speaker _Left channel
J27	Speaker_ Right channel
J31	PWM
J22	MIPI-CSI

J23	MIPI-CSI
BT1	RTC battery
U17	PCIE3.0
J21	MIPI-CSI
J20	MIPI-CSI
J18	MIPI-DSI
J19	MIPI-DSI
J14	eDP
J17	Backlight
J16	Backlight volage_ DIP selection
SW7	ADC Button
SW5	ADC Button
SW4	ADC Button
SW2	Recovery Button
J11	M.2 M-KEY(PCIE2.0)
J9	M.2 B-KEY (USB3.0)
S1	SIM socket

3.2.PIN Definition

J1A: PIN Definition on SOM module

Multiplexing GPIO	Signal Name	PIN#	PIN#	Single Name	Multiplexing GPIO
		1	2		
		3	4		
	GND	5	6	GND	
	MIPI_CSI0_RX_D3P	7	8	MIPI_CSI1_RX_D3 N	
	MIPI_CSI0_RX_D3N	9	10	MIPI_CSI1_RX_D3P	
	GND	11	12	GND	
	MIPI_CSI0_RX_D2P	13	14	MIPI_CSI1_RX_D2 N	
	MIPI_CSI0_RX_D2N	15	16	MIPI_CSI1_RX_D2P	
	GND	17	18	GND	
	MIPI_CSI0_RX_CLK0P	19	20	MIPI_CSI1_RX_CL K0N	
	MIPI_CSI0_RX_CLK0N	21	22	MIPI_CSI1_RX_CL K0P	
	GND	23	24	GND	
	MIPI_CSI0_RX_D1P	25	26	MIPI_CSI1_RX_D1 N	
	MIPI_CSI0_RX_D1N	27	28	MIPI_CSI1_RX_D1P	
	GND	29	30	GND	
	MIPI_CSI0_RX_D0P	31	32	MIPI_CSI1_RX_D0 N	

	MIPI_CSI0_RX_D0N	33	34	MIPI_CSI1_RX_D0P	
	GND	35	36	GND	
GPIO3_A5_d	GMAC1_RXCLK	37	38	PCIE20X1_2_nCLK REQ	GPIO3_C7_u
GPIO3_B1_d	GMAC1_RXDV	39	40	PCIE20X1_2_nWAK E	GPIO3_D0_u
GPIO3_A7_u	GMAC1_RXD0	41	42	PCIE20X1_2_nPERS T	GPIO3_D1_d
GPIO3_B0_u	GMAC1_RXD1	43	44	UART9_nCTS	GPIO3_D3_d
GPIO3_A2_u	GMAC1_RXD2	45	46	UART9_nRTS	GPIO3_D2_d
GPIO3_A3_u	GMAC1_RXD3	47	48	UART9_RXD	GPIO3_D4_d
GPIO3_A4_d	GMAC1_TXCLK	49	50	UART9_TXD	GPIO3_D5_d
GPIO3_B5_u	GMAC1_TXEN	51	52	GPIO_WL_nDISAB LE1	GPIO3_C5_u
GPIO3_B3_u	GMAC1_TXD0	53	54	GPIO_WL_nDISAB LE2	GPIO3_C4_u
GPIO3_B4_u	GMAC1_TXD1	55	56	GPIO_ENET1_nRST	GPIO3_C6_u
GPIO3_A0_u	GMAC1_TXD2	57	58	GPIO_ENET1_nINT	GPIO3_B2_d
GPIO3_A1_u	GMAC1_TXD3	59	60	GND	
	GND	61	62	GPIO_ENET0_nRST	GPIO3_A6_d
GPIO3_C2_d	GMAC1_MDC	63	64	GPIO_ENET0_nINT	GPIO3_B6_d
GPIO3_C3_d	GMAC1_MDIO	65	66	GND	
	GND	67	68	GPIO_RS485_DIR	GPIO3_B7_d
GPIO2_B0_u	GMAC0_RXCLK	69	70	UART7_TXD	GPIO3_C0_d
GPIO4_C2_d	GMAC0_RXDV	71	72	UART7_RXD	GPIO3_C1_d

GPIO2_C1_d	GMAC0_RXD0	73	74	GPIO_CAM_nRST	GPIO2_B4_u
GPIO2_C2_d	GMAC0_RXD1	75	76	GPIO_CAM4_PWD N	GPIO2_B5_u
GPIO2_A6_u	GMAC0_RXD2	77	78	GPIO_CAM3_PWD N	GPIO2_C4_d
GPIO2_A7_u	GMAC0_RXD3	79	80	GPIO_CAM2_PWD N	GPIO2_C5_d
GPIO2_B3_d	GMAC0_TXCLK	81	82	GPIO_CAM1_PWD N	GPIO2_C6_d
GPIO2_C0_d	GMAC0_TXEN	83	84	GND	
GPIO2_B6_d	GMAC0_TXD0	85	86	GPIO_EXT_PWR_E N	GPIO2_C3_d
GPIO2_B7_d	GMAC0_TXD1	87	88	GPIO_RUN_LED	GPIO4_C3_d
GPIO2_B1_u	GMAC0_TXD2	89	90	GND	
GPIO2_B2_u	GMAC0_TXD3	91	92	GPIO_5G_ON_OFF	GPIO0_A0_d
	GND	93	94	SDMMC_DET_L	
GPIO4_C5_d	GMAC0_MDIO	95	96	GPIO_5G_W_DIS	GPIO0_B0_z
GPIO4_C4_d	GMAC0_MDC	97	98	GPIO_5G_RST	GPIO0_B3_z
	GND	99	100	GND	

J1B: PIN Definition on SOM module

Multiplexing GPIO	Signal Name	PIN#	PIN#	Signal Name	Multiplexing GPIO
	VCC_SYS_4V0	1	2	VCC_SYS_4V0	
	VCC_SYS_4V0	3	4	VCC_SYS_4V0	
	VCC_SYS_4V0	5	6	VCC_SYS_4V0	

	VCC_SYS_4V0	7	8	VCC_SYS_4V0	
	VCC_SYS_4V0	9	10	VCC_SYS_4V0	
	VCC_SYS_4V0	11	12	VCC_SYS_4V0	
	VCC_SYS_4V0	13	14	VCC_SYS_4V0	
	GND	15	16	GND	
	GND	17	18	GND	
	GND	19	20	GND	
	GND	21	22	GND	
	GND	23	24	VCC_ADC_1V8	
	SYS_nRST	25	26	VCC_SYS_1V8	
	PMIC_PWRON	27	28	VCC_SYS_3V3	
		29	30	VCC_SYS_3V3	
	GND	31	32	GND	
	MIPI_DPHY0_RX_D3P	33	34	MIPI_DPHY0_TX_D 3P	
	MIPI_DPHY0_RX_D3N	35	36	MIPI_DPHY0_TX_D 3N	
	MIPI_DPHY0_RX_D2P	37	38	MIPI_DPHY0_TX_D 2P	
	MIPI_DPHY0_RX_D2N	39	40	MIPI_DPHY0_TX_D 2N	
	GND	41	42	GND	
	MIPI_DPHY0_RX_CLKP	43	44	MIPI_DPHY0_TX_C LKP	
	MIPI_DPHY0_RX_CLKN	45	46	MIPI_DPHY0_TX_C LKN	

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	GND	47	48	GND	
	MIPI_DPHY0_RX_D1P	49	50	MIPI_DPHY0_TX_D 1P	
	MIPI_DPHY0_RX_D1N	51	52	MIPI_DPHY0_TX_D 1N	
	MIPI_DPHY0_RX_D0P	53	54	MIPI_DPHY0_TX_ D0P	
	MIPI_DPHY0_RX_D0N	55	56	MIPI_DPHY0_TX_ D0N	
	GND	57	58	GND	
	MIPI_DPHY1_RX_D3P	59	60	MIPI_DPHY1_TX_D 3P	
	MIPI_DPHY1_RX_D3N	61	62	MIPI_DPHY1_TX_D 3N	
	MIPI_DPHY1_RX_D2P	63	64	MIPI_DPHY1_TX_D 2P	
	MIPI_DPHY1_RX_D2N	65	66	MIPI_DPHY1_TX_D 2N	
	GND	67	68	GND	
	MIPI_DPHY1_RX_CLKP	69	70	MIPI_DPHY1_TX_C LKP	
	MIPI_DPHY1_RX_CLKN	71	72	MIPI_DPHY1_TX_C LKN	
	GND	73	74	GND	
	MIPI_DPHY1_RX_D1P	75	76	MIPI_DPHY1_TX_D 1P	

	MIPI_DPHY1_RX_D1N	77	78	MIPI_DPHY1_TX_D1N	
	MIPI_DPHY1_RX_D0P	79	80	MIPI_DPHY1_TX_D0P	
	MIPI_DPHY1_RX_D0N	81	82	MIPI_DPHY1_TX_D0N	
	GND	83	84	GND	
GPIO4_B2_u	TYPEC1_SBU1_DC	85	86	TYPEC0_SBU1_DC	GPIO4_B0_d
GPIO4_B3_u	TYPEC1_SBU2_DC	87	88	TYPEC0_SBU2_DC	GPIO4_B1_u
		89	90	GND	
	SARADC_IN1_RECOVERY	91	92	TYPEC0_SSTX2N	
	SARADC_IN0_BOOT	93	94	TYPEC0_SSTX2P	
	GND	95	96	GND	
	TYPEC0_SBU2	97	98	TYPEC0_SSRX2P	
	TYPEC0_SBU1	99	100	TYPEC0_SSRX2N	

J1C:PIN Definition on SOM module

Multiplexing GPIO	Signal Name	PIN#	IN#	Signal Name	Multiplexing GPIO
	USB30_2_SSRXN	1	2	PCIE30_PORT0_RX0P	
	USB30_2_SSRXP	3	4	PCIE30_PORT0_RX0N	
	GND	5	6	GND	
	USB30_2_SSTXN	7	8	PCIE30_PORT0_RX1P	
	USB30_2_SSTXP	9	10	PCIE30_PORT0_RX1N	
	GND	11	12	GND	

		13	14	PCIE30_PORT0_REFCL KN_IN	
		15	16	PCIE30_PORT0_REFCL KP_IN	
	GND	17	18	GND	
	PCIE20_0_RXP	19	20	PCIE30_PORT0_TX0N	
	PCIE20_0_RXN	21	22	PCIE30_PORT0_TX0P	
	GND	23	24	GND	
	PCIE20_0_TXN	25	26	PCIE30_PORT0_TX1N	
	PCIE20_0_TXP	27	28	PCIE30_PORT0_TX1P	
	GND	29	30	GND	
	PCIE20_0_REFCLKP	31	32	PCIE30_PORT1_RX0P	
	PCIE20_0_REFCLKN	33	34	PCIE30_PORT1_RX0N	
	GND	35	36	GND	
	PCIE20_1_TXP	37	38	PCIE30_PORT1_RX1P	
	PCIE20_1_TXN	39	40	PCIE30_PORT1_RX1N	
	GND	41	42	GND	
	PCIE20_1_RXP	43	44	PCIE30_PORT1_TX0P	
	PCIE20_1_RXN	45	46	PCIE30_PORT1_TX0N	
	GND	47	48	GND	
	PCIE20_1_REFCLKP	49	50	PCIE30_PORT1_TX1P	
	PCIE20_1_REFCLKN	51	52	PCIE30_PORT1_TX1N	
	GND	53	54	GND	
GPIO0_D0_d	I2C6_SCL_1V8	55	56	PCIE30_PORT1_REFCL KP_IN	

GPIO0_C7_d	I2C6_SDA_1V8	57	58	PCIE30_PORT1_REFCL	
				KN_IN	
GPIO0_C0_d	PWM1_OUT	59	60	GND	
GPIO0_B7_d	PWM0_OUT	61	62	GPIO_TYPEC0_nINT	GPIO0_C6_u
GPIO0_C4_d	PWM2_OUT	63	64	GPIO_TYPEC1_nINT	GPIO0_D3_u
GPIO0_C5_u	PWM4_OUT	65	66	GPIO_WDT_EN	GPIO1_A7_u
	UART2_RXD	67	88	GPIO_WDT_FEED	GPIO1_A4_d
	UART2_TXD	69	70	HDMI_TX0_HPD	GPIO1_A5_d
	GND	71	72	GMAC0_RXD3	GPIO1_A6_d
GPIO1_C0_z	I2C3_SDA_1V8	73	74	GPIO1_A6	GPIO1_B0_u
GPIO1_C1_z	I2C3_SCL_1V8	75	76	GPIO1_B1	GPIO1_B1_d
	GPIO_EXPIO_nINT	77	78	GPIO1_B2	GPIO1_B2_d
	GPIO_BT_nINT	79	80	PCIE30X1_0_nCLKREQ	GPIO1_B5_u
	GPIO_HP_DET	81	82	PCIE30X1_0_nWAKE	GPIO1_B3_d
GPIO1_C2_d	I2S0_MCLK	83	84	PCIE30X1_0_nPERST	GPIO1_B4_u
GPIO1_C3_d	I2S0_SCLK	85	86	I2C4_SCL_3V3	GPIO1_A3_d
GPIO1_C5_d	I2S0_LRCK	87	88	I2C4_SDA_3V3	GPIO1_A2_d
GPIO1_C7_d	I2S0_SDO0	89	90	I2C2_SCL_3V3	GPIO1_A1_d
GPIO1_D4_d	I2S0_SDI0	91	92	I2C2_SDA_3V3	GPIO1_A0_d
GPIO1_D3_d	GPIO_AMP_SD	93	94	HDMI_RX_CEC	GPIO1_B7_u
	GPIO_HDMI_RX_DET	95	96	HDMI_RX_HPDOOUT	GPIO1_B6_u
GPIO1_D1_d	I2C7_SDA_1V8	97	98	HDMI_RX_SDA	GPIO1_D7_u
GPIO1_D0_d	I2C7_SCL_1V8	99	100	HDMI_RX_SCL	GPIO1_D6_u

J1D:PIN Definition on SOM module

Multiplexing GPIO	Signal Name	PIN#	PIN#	Signal Name	Multiplexing GPIO
	TYPEC0_OTG_DM	1	2	TYPEC0_SSTX1N	
	TYPEC0_OTG_DP	3	4	TYPEC0_SSTX1P	
	GND	5	6	GND	
		7	8	TYPEC0_SSRX1P	
		9	10	TYPEC0_SSRX1N	
	GND	11	12	GND	
	TYPEC1_SBU2	13	14	TYPEC1_SSTX2N	
	TYPEC1_SBU1	15	16	TYPEC1_SSTX2P	
	GND	17	18	GND	
	TYPEC1_OTG_DM	19	20	TYPEC1_SSRX2P	
	TYPEC1_OTG_DP	21	22	TYPEC1_SSRX2N	
	GND	23	24	GND	
	USB2_HOST1_DM	25	26	TYPEC1_SSTX1N	
	USB2_HOST1_DP	27	28	TYPEC1_SSTX1P	
	GND	29	30	GND	
	USB2_HOST0_DM	31	32	TYPEC1_SSRX1P	
	USB2_HOST0_DP	33	34	TYPEC1_SSRX1N	
	GND	35	36	GND	
	HDMI_TX0_D2P	37	38	EDP_TX1_D2P	
	HDMI_TX0_D2N	39	40	EDP_TX1_D2N	
	GND	41	42	GND	
	HDMI_TX0_D1P	43	44	EDP_TX1_D1P	
	HDMI_TX0_D1N	45	46	EDP_TX1_D1N	
	GND	47	48	GND	

	HDMI_TX0_D0P	49	50	EDP_TX1_D0P	
	HDMI_TX0_D0N	51	52	EDP_TX1_D0N	
	GND	53	54	GND	
	HDMI_TX0_D3P	55	56	EDP_TX1_D3P	
	HDMI_TX0_D3N	57	58	EDP_TX1_D3N	
	GND	59	60	GND	
	HDMI_TX0_SBDP	61	62	EDP_TX1_AUXP	
	HDMI_TX0_SBDN	63	64	EDP_TX1_AUXN	
	GND	65	66	GND	
GPIO4_B7_u	HDMI_TX0_SCL	67	68	GPIO_LCD2_TP_nI NT	GPIO4_A1_d
GPIO4_C0_u	HDMI_TX0_SDA	69	70	GPIO_LCD2_TP_nR ST	GPIO4_A0_d
GPIO4_C1_d	HDMI_TX0_CEC	71	72	GPIO_LCD1_TP_nR ST	GPIO4_A2_d
	GPIO_HDMI_TX0_ON	73	74	UART0_TXD	GPIO4_A3_d
	GPIO_LCD_nRST	75	76	UART0_RXD	GPIO4_A4_d
	GPIO_LCD_BL_EN	77	78	GPIO_LCD1_TP_nI NT	
GPIO4_A6_d	UART3_RXD	79	80	GND	
GPIO4_A5_d	UART3_TXD	81	82	HDMI_RX_D2P	
	GND	83	84	HDMI_RX_D2N	
GPIO4_D3_u	SDMMC_D3	85	86	HDMI_RX_D1P	
GPIO4_D2_u	SDMMC_D2	87	88	HDMI_RX_D1N	
GPIO4_D1_u	SDMMC_D1	89	90	HDMI_RX_D0P	

GPIO4_D0_u	SDMMC_D0	91	92	HDMI_RX_D0N	
GPIO4_D4_u	SDMMC_CMD	93	94	GND	
	GND	95	96	HDMI_RX_CLKP	
GPIO4_D5_d	SDMMC_CLK	97	98	HDMI_RX_CLKN	
	GND	99	100	GND	

J33: Power

PIN#	Signal Name
1	GND
2	VCC_EXT_PWR

J30: RS485

PIN#	Signal Name
1	RS485_B
2	RS485_A
3	GND

J28/J29: RS232

PIN#	Signal Name
1	TXD
2	RXD
3	GND

J16: Backlight Voltage_ Jumper

Signal Name	PIN#	PIN#	Signal Name
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VCC_EXT_PWR	1	2	VCC_LCD3_BL
VCC_EXT_12V0	3	4	VCC_LCD3_BL
VCC_EXT_5V0	5	6	VCC_LCD3_BL

J18/J19: MIPI-DSI

PIN#	Signal Name
1	TP_I2C_SDA
2	TP_I2C_SCL
3	TP_nRST
4	TP_nINT
5	BL_EN
6	VCC_EXT_5V0
7	VCC_EXT_5V0
8	VCC_EXT_5V0
9	VCC_EXT_5V0
10	GND
11	GND
12	GND
13	NC
14	LCD_nRST
15	NC
16	GND
17	LCD_MIPI_D3_N
18	LCD_MIPI_D3_P
19	GND

20	LCD_MIPI_D0_N
21	LCD_MIPI_D0_P
22	GND
23	LCD_MIPI_CLK_N
24	LCD_MIPI_CLK_P
25	GND
26	LCD_MIPI_D1_N
27	LCD_MIPI_D1_P
28	GND
29	LCD_MIPI_D2_N
30	LCD_MIPI_D2_P
31	GND
32	LCD_BL_PWM
33	GND
34	GND
35	GND
36	NC
37	VCC_EXT_12V0
38	VCC_EXT_12V0
39	VCC_EXT_12V0
40	VCC_EXT_12V0

J20/J21/J22/J23: MIPI-CSI

PIN#	Signal Name
1	GND

2	MIPI_CLKP
3	MIPI_CLKN
4	GND
5	MIPI_D2P
6	MIPI_D2N
7	GND
8	MIPI_D0P
9	MIPI_D0N
10	GND
11	MIPI_D3P
12	MIPI_D3N
13	GND
14	MIPI_D1P
15	MIPI_D1N
16	GND
17	VCC_CAM_1V8
18	GND
19	CAM_PWDN
20	CAM_nRST
21	CAM_I2C_SDA
22	CAM_I2C_SCL
23	VCC_CAM_1V2
24	GND
25	CAM_MCLK
26	GND

27	VCC_CAM_1V8
28	GND
29	VCC_CAM_2V8
30	VCC_CAM_2V8

J15: I2C (TP)

PIN#	Signal Name
1	VCC_TP_3V3
2	TP_I2C_SCL
3	TP_I2C_SDA
4	TP_nINT
5	TP_nRST
6	GND

J26: Speaker_Line Out

PIN#	Signal Name
1	AUD_AMP_OUTPL
2	AUD_AMP_OUTNL

J27:Speaker_Line Out

PIN#	Signal Name
1	AUD_AMP_OUTPR
2	AUD_AMP_OUTNR

J24:MIC

PIN#	Signal Name
1	AUD_MIC+
2	AUD_MIC-

J31:PWM

PIN#	Signal Name
1	VCC_EXT_12V0
2	PWM4_OUT

J14: EDP

Signal Name	PIN#	PIN#	Signal Name
VCC_EDP_LCD	2	1	VCC_EDP_LCD
VCC_EDP_LCD	4	3	VCC_EDP_LCD
EDP_TX1_D0N	6	5	EDP_TX1_D0P
EDP_TX1_D1N	8	7	EDP_TX1_D1P
EDP_TX1_D2N	10	9	EDP_TX1_D2P
EDP_TX1_D3N	12	11	EDP_TX1_D3P
GND	14	13	GND
EDP_TX1_AUXN	16	15	EDP_TX1_AUXP
GND	18	17	GND
EDP_nRST	20	19	EDP_HPD

J10: M.2 E-KEY socket

Signal Name	PIN#	PIN#	Signal Name
GND	1	2	VCC_WL_3V3
NC	3	4	VCC_WL_3V3

NC	5	6	NC
GND	7	...	NC
NC	...	18	GND
NC	19	20	GPIO_BT_nINT
NC	21	22	BT_UART_TXD
GND	23	...	
	...	32	BT_UART_RXD
GND	33	34	BT_UART_nRTS
PCIE20_0_TXP	35	36	BT_UART_nCTS
PCIE20_0_TXN	37	38	NC
GND	39	40	NC
PCIE20_0_RXP	41	42	BT_WAKE
PCIE20_0_RXN	43	44	NC
GND	45	46	NC
PCIE20_0_REFCLKP	47	48	NC
PCIE20_0_REFCLKN	49	50	CLK_32K_OUT
GND	51	52	PCIE20X1_2_nPERST
PCIE20X1_2_nCLKREQ	53	54	GPIO_WL_nDISABLE2
PCIE20X1_2_nWAKE	55	56	GPIO_WL_nDISABLE1
GND	57	58	NC
GND	59	60	NC
NC	61	62	NC
GND	63	64	GND
NC	65	66	NC
NC	67	68	NC

GND	69	70	NC
NC	71	72	VCC_WL_3V3
NC	73	74	VCC_WL_3V3
GND	75		

U17: PCIE3.0 Socket

Signal Name	PIN#	PIN#	Signal Name
VCC_PCIE30_SLOT_12V0	B1	A1	GND
VCC_PCIE30_SLOT_12V0	B2	A2	VCC_PCIE30_SLOT_12V0
VCC_PCIE30_SLOT_12V0	B3	A3	VCC_PCIE30_SLOT_12V0
GND	B4	A4	GND
NC	B5	A5	NC
NC	B6	A6	NC
GND	B7	A7	NC
VCC_PCIE30_SLOT_3V3	B8	A8	NC
NC	B9	A9	VCC_PCIE30_SLOT_3V3
VCC_PCIE30_SLOT_3V3	B10	A10	VCC_PCIE30_SLOT_3V3
PCIE30X4_nWAKE	B11	A11	PCIE30X4_nPERST
PCIE30X4_nCLKREQ	B12	A12	GND
GND	B13	A13	PCIE30_REFCLKP_SLOT
PCIE30_PORT0_TX0P	B14	A14	PCIE30_REFCLKN_SLOT
PCIE30_PORT0_TX0N	B15	A15	GND
GND	B16	A16	PCIE30_PORT0_RX0P
GPIO_PCIE30X4_nHPD	B17	A17	PCIE30_PORT0_RX0N
GND	B18	A18	GND

PCIE30_PORT0_TX1P	B19	A19	NC
PCIE30_PORT0_TX1N	B20	A20	GND
GND	B21	A21	PCIE30_PORT0_RX1P
GND	B22	A22	PCIE30_PORT0_RX1N
PCIE30_PORT1_TX0P	B23	A23	GND
PCIE30_PORT1_TX0N	B24	A24	GND
GND	B25	A25	PCIE30_PORT1_RX0P
GND	B26	A26	PCIE30_PORT1_RX0N
PCIE30_PORT1_TX1P	B27	A27	GND
PCIE30_PORT1_TX1N	B28	A28	GND
GND	B29	A29	PCIE30_PORT1_RX1P
NC	B30	A30	PCIE30_PORT1_RX1N
VCC_PCIE30_SLOT_3V3	B31	A31	GND
GND	B32	A32	NC

J11: M.2 M-KEY socket

Signal Name	PIN#	PIN#	Signal Name
GND	1	2	VCC_SSD_3V3
GND	3	4	VCC_SSD_3V3
NC	5	6	NC
NC	7	8	NC
GND	9	10	VCC_SSD_3V3
NC	11	12	VCC_SSD_3V3
NC	13	14	VCC_SSD_3V3
GND	15	16	VCC_SSD_3V3

NC	17	18	VCC_SSD_3V3
NC	19	20	NC
GND	21	22	NC
NC	23	24	NC
NC	25	26	NC
GND	27	28	NC
NC	29	30	NC
NC	31	32	NC
GND	33	34	NC
NC	35	36	NC
NC	37	38	NC
GND	39	40	NC
PCIE20_1_RXN	41	42	NC
PCIE20_1_RXP	43	44	5G_PCIE_nPERST
GND	45	46	5G_PCIE_nCLKREQ
PCIE20_1_TXN	47	48	5G_PCIE_nPEWAKE
PCIE20_1_TXP	49	50	NC
GND	51	52	NC
PCIE20_1_REFCLKN	53	54	NC
PCIE20_1_REFCLKP	55	56	NC
GND	57	58	NC
NC	...	...	NC
NC	67	68	NC
NC	69	70	VCC_SSD_3V3
GND	71	72	VCC_SSD_3V3

GND	73	74	VCC_SSD_3V3
GND	75		

J9: M.2 B-KEY socket

Signal Name	PIN#	PIN#	Signal Name
NC	1	2	VCC_5G_3V8
GND	3	4	VCC_5G_3V8
GND	5	6	5G_ON_OFF
USB2_HOST1_DP	7	8	GPIO_5G_W_DIS
USB2_HOST1_DM	9	10	VCC_5G_3V8
GND	11	...	STD B-KEY
STD B-KEY	...	20	NC
NC	21	22	NC
VCC_EXT_1V8	23	24	NC
NC	25	26	NC
GND	27	28	NC
USB30_2_SSRXN	29	30	USIM_nRST
USB30_2_SSRXP	31	32	USIM_CLK
GND	33	34	USIM_DATA
USB30_2_SSTXN	35	36	VCC_USIM
USB30_2_SSTXP	37	38	VCC_EXT_1V8
GND	39	40	NC
NC	41	42	NC
NC	43	44	NC
GND	45	46	NC

NC	47	48	NC
NC	49	50	NC
GND	51	52	NC
NC	53	54	NC
NC	55	56	NC
GND	57	58	NC
NC	59	60	NC
NC	61	62	NC
NC	63	64	NC
NC	65	66	USIM_DET
GPIO_5G_RST	67	68	NC
NC	69	70	VCC_5G_3V8
GND	71	72	VCC_5G_3V8
GND	73	74	VCC_5G_3V8
NC	75		

J5: USB-OTG (HOST/Device)

PIN#	Signal Name
1	USB3_OTG0_ID
2	VCC_PMU_1V8

S1: SIM Socket (Bottom Side)

PIN#	Signal Name
1	VCC_USIM
2	USIM_nRST

3	USIM_DET
4	USIM_CLK
5	GND
6	NC
7	USIM_DATA

IV. Size & Structure

Unit:mm, if needs the size of the board to board receptacle, please email: supports@qiyangtech.com

4.1.Size of SOM Module

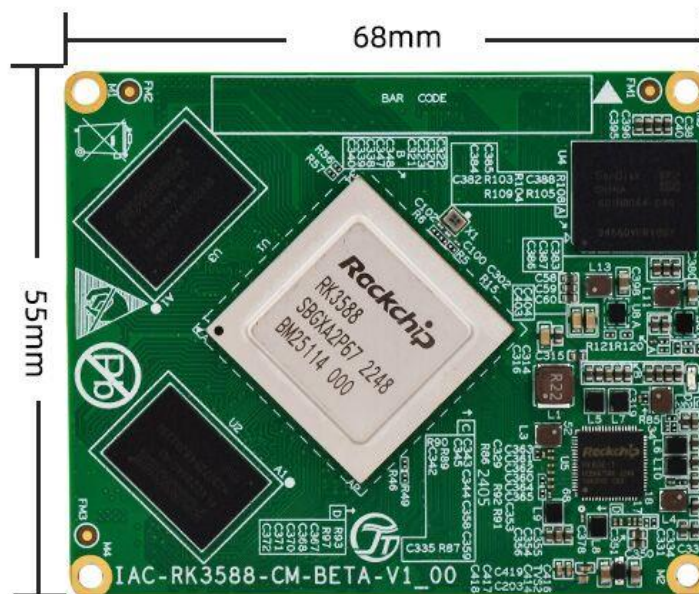


Figure 5

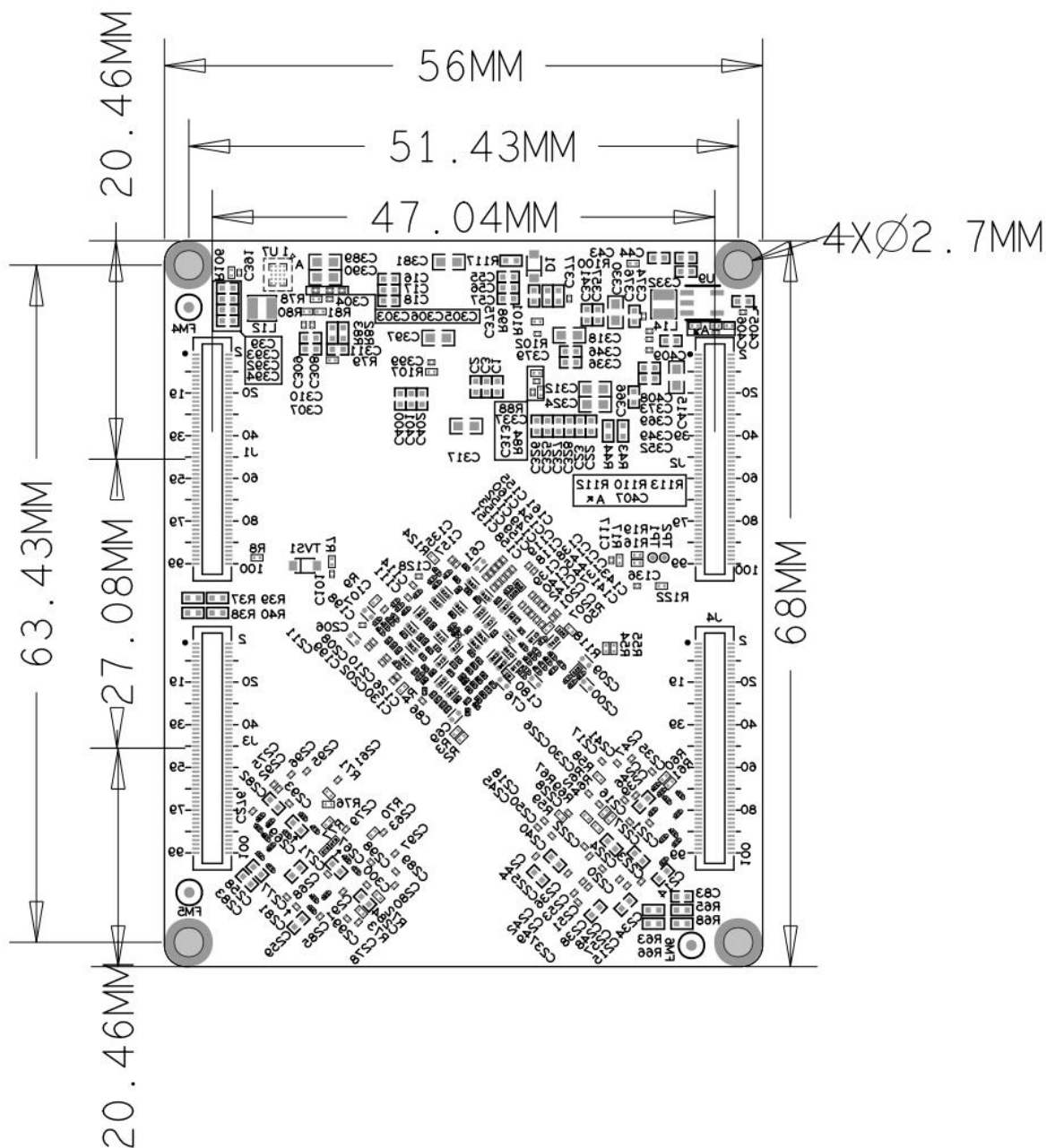


Figure 6

4.2.Size of Carrier Board

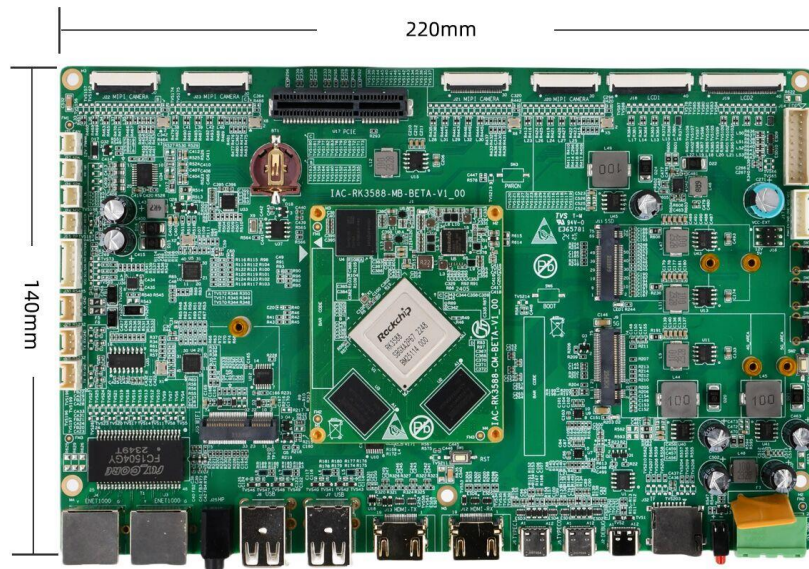


Figure 7

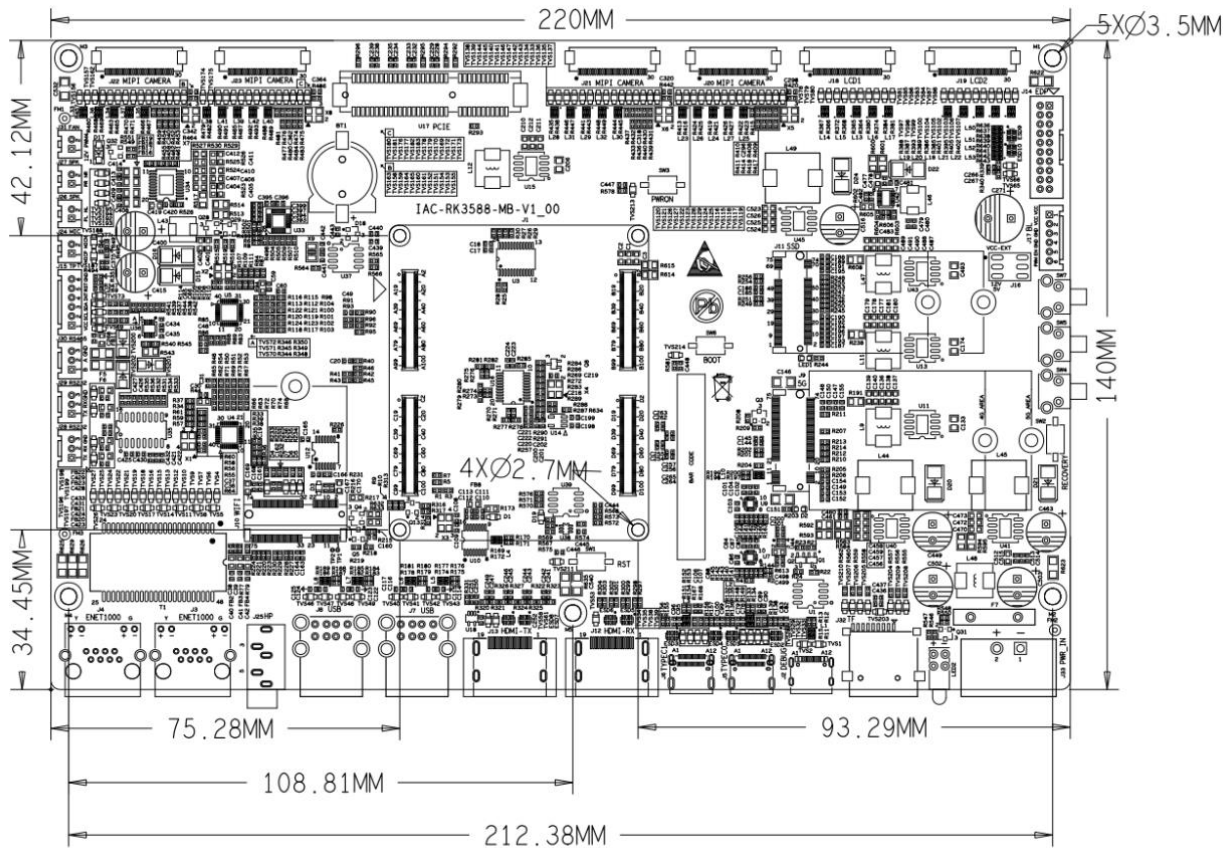


Figure 8

V. Connection between SOM module and Carrier Board

Pay attention on the location of the SOM module :(Refer to below picture)

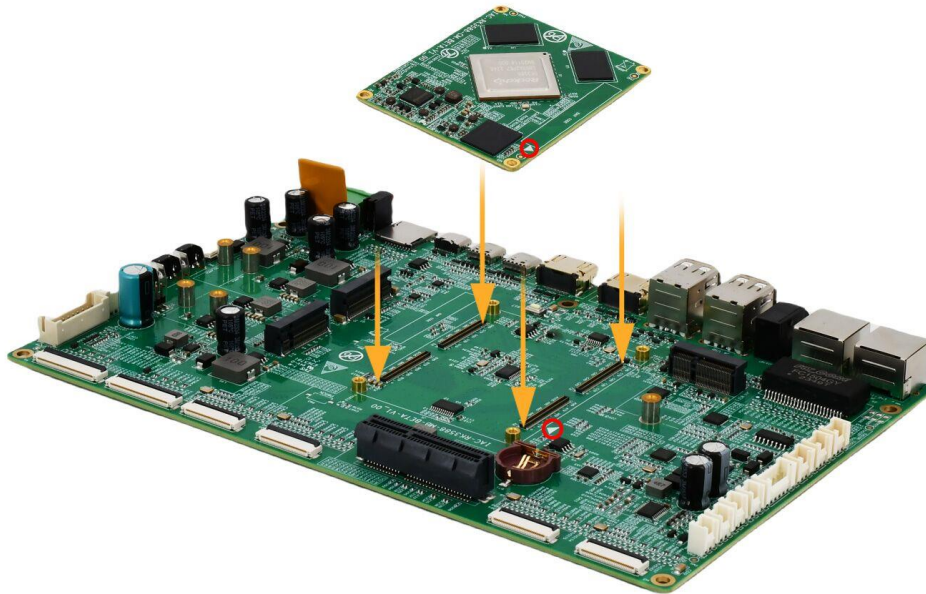


Figure 9

VI. Electricity

Item	Features
Operational Temperature	0℃ ~ +70℃ (-20℃ ~ +85℃ optional)
Storage Temperature	-10℃ ~ +70℃
Humidity	10%~90%, non-condensation
Dimensions of SOM	68mm*55mm, 10-layer high precision immersion gold process
Dimensions of Carrier Board	220mm*140mm, 6-layer high precision immersion gold process
Power consumption of SOM module	To be continued
Power consumption of whole board	To be continued
Power Supply	DC12V/2.5A

VII. Software Description

IAC-RK3568-Kit supports Debian/Android OS.

It introduces Debian Linux and Android environment setup and steps detailly for IAC-RK3588-KIT on ***IAC-RK3568-Kit User Manual***.

VIII. Remark

Under these circumstances, we do not offer repair for free:

- Over warranty time;
- Do not attach purchase receipt;
- Liquid inlet, damp or mold;
- Malfunction and damage is not due to product quality but drops, intense shaking, arbitrarily modify, disoperation after purchase;
- Damage of force majeure.

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We accept batch order. We can offer technical support and service.

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