SMARC-IMX8MP-KIT Hardware Manual

Ver.#:1.10

2025.7

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Information updates

2023. Information updates

Product-related manuals and datasheets are constantly being improved and updated; please ensure that they are up-to-date when you use them.

2.Update notice

Qiyang's newest product information and news updates will be released through the WeChat official account, please pay attention!

Version Record

Version	Hardware Platform	Description	Date
V1.0	SMARC-MB-V1_00 SMARC-IMX8MP-CM-V1_00	2024-11	Initial Version
V1.10	SMARC-MB-V1_00 SMARC-IMX8MP-CM-V1_20	2025-7	WLAN Module Change

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Notice: This manual introduces the hardware interface of the SMARC-IMX8MP-Kit Development Kit.

Ⅰ. Preface

1.1.Company Profile

Zhejiang Qiyang Intelligent Technology Co., Ltd., established in 2007, which locates in Hangzhou, Zhejiang, PRC. It is a high-end technological enterprise that specializes in exploitation, fabrication, and selling embedded computer mainboards . With 10 years of experiences, Qiyang has established the completed service chain from the design concept to mass production successfully.

The R&D team is organized by 30 more technical engineers. Qiyang focus on providing functional embedded hardware, software tool and customization solutions. It has been applied to Industrial Control, Internet of Things, New Retail, Smart Medical, Electricity Device, Environmental Surveillance, Charging Pile etc.

With the growth of the business, Qiyang has set up an SMT factory in Zhuji, Zhejiang province, which is 5000 ㎡, with a 2xSMT production line. The SMT factory performs the ISO9001 Quality Management System strictly. Relying on the solid production ability, the SMT factory's annual capacity is about a million sets, which totally guarantee the delivery date.

Qiyang has a thorough sales marketing network, professional sales ,and after-sales team to provide full technical support and service. The business has spread over 120 countries and areas, it helps the clients to introduce the products into the market efficiently and successfully.The combination and extension of research and development, production capacity, and market, that provide a solid foundation for Qiyang to provide specialized, globalized embedded hardware and software.

We offer:

I.Software/Hardware Mainboard

Based on the CPU solution from NXP,Rockchip,MTK,Renesas,TI,Atmel,Cirrus Logic etc, Qiyang provides the ARM development kit/system on module/industrial board and periphery products, paired tools and software for the user do further exploitation.

2.Customization Service

Fully taking the advantage of the technical accumulation on the ARM platform and Linux, Android, Ubuntu OS, Qiyang provides the efficient OEM/ODM service to the users.

Sincerely thanks for using Qiyang's product, we will try our best to offer you the technical supports!

1.2.SMARC-IMX8MP-KIT Development Kit Use Suggestion:

1. Please read the instructions firstly, before using the SMARC-IMX8MP-Kit development Kit.

2. Before using, please check the packing list and see whether there is a missing file in the CD;

3. Please understand the basic structure and composition of SMARC-IMX8MP-CM SOM, including the

hardware resource allocation etc.;

4. If you need to develop on Debian Linux system and burn program into the development board, in addition,

we also suggest reading another documentation ***SMARC-IMX8MP-Kit Linux User Manual;***

5. If you need to develop on Android system and burn program into the development board, in addition, we

also suggest reading another documentation ***SMARC-IMX8MP-Kit Android User Manual;***

6.Accept batch order.

II. Introduction

2.1. Overview

SMARC-IMX8MP-KIT Development Board, it adopts NXP IMX8MPlus series processor, the i.MX 8M Plus family focuses on neural processing unit (NPU) and vision system, advance multimedia, and industrial automation with high reliability.

The i.MX 8M Plus is a powerful quad Arm® Cortex®-A53 processor with speed up to 1.8 GHz integrated with an NPU of 2.3 TOPS that greatly accelerate machine learning inference. The vision engine is composed of two camera inputs and an HDR-capable Image.Signal Processor (ISP) capable of 375 MPixels/s.The advanced multimedia capabilities include 1080p60 video encode and decode H.265 and H.264. A 3D and 2D graphic acceleration supporting 1 GPixel/s, OpenVG 1.1, Open GL ES3.1, Vulkan, and Open CL 1.2 FP. Multiple audio and microphone interfaces for Immersive Audio and Voice systems.

For industrial applications, real time control is enabled by an integrated 800 MHz Arm® Cortex®-M7. Robust control networks are possible via CAN-FD interfaces. And a dual Gb Ethernet, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency. High industrial system reliability for safety is leveraged by DRAM Inline ECC as well as ECC support on internal software-accessible SRAMs.

Block Diagram of IMX8M Plus:

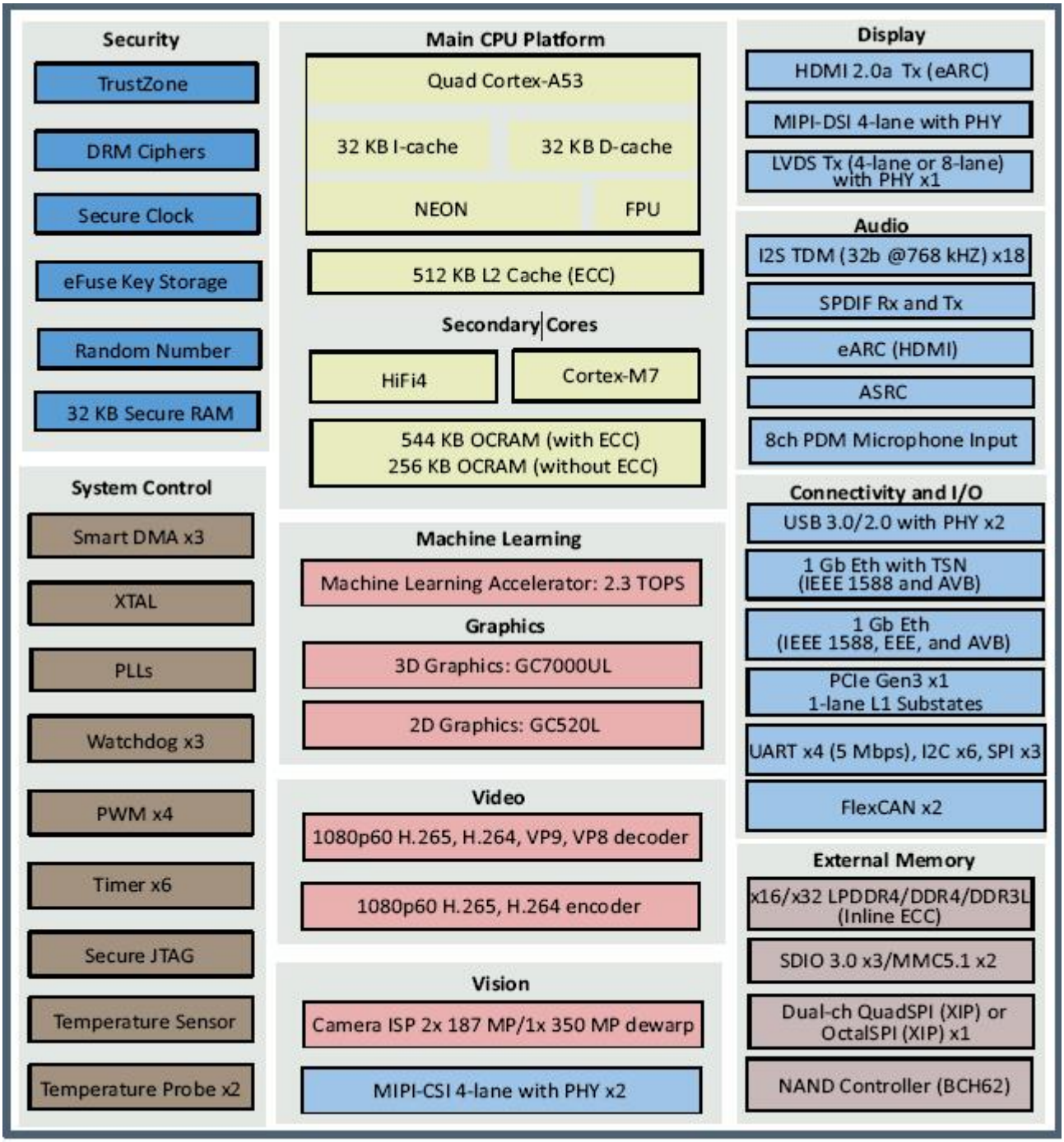

Figure 1

Detailed Parameters of IMX8M Plus

CORE	CPU	● Quad Cortex®-A53 processors, frequency up to 1.8 GHz ● 32 KB L1 Instruction Cache，32 KB L1 Data Cache ● 512 KB unified L2 cache ● Support of 64-bit Armv8-A architecture
	MCU	● Arm®Cortex®-M7 800MHz ● 32 KB L1 Instruction Cache，32 KB L1 Data Cache ● 256 KB TCM contains DTCM，ITCM（128KB+128KB) 256 KB tightly coupled memory (TCM) (128KB+128KB)
Storage	On-chip Memory	● Boot ROM (256 KB) ● On-chip RAM (512KB + 32KB) with ECC support
	External Storage	● 16/32-bit DRAM Interface:LPDDR4-4000,DDR4-3200,DDR3L-1600 ● 8-bit NandFlash, including support for RAW MLC/SLC devices, BCH ECC up to 64bit, and ONFi3.2 compliance (clock rates up to 100MHz and data rates up to 200MB/Sec.) ● EMMC 5.1 FLASH ● SPI NOR FLASH ● FlexSPI Flash with support for XIP (for Cortex®-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices. It also supports both Serial NOR and Serial NAND flash using the FlexSPI.
On-chip Unit	GPU	● GC7000UL with OpenCL and Vulkan support ● Supports OpenGL ES 1.1, 2.0, 3.0, OpenCL 1.2, Vulkan ● GC520L for 2D acceleration
	NPU	● 2.3 TOP/s
	ISP	● It includes 2xISP, to support dual camera input ● ISP with 375 Mpixel/s, to support 12MP@30fps, 4kp45, or 2x 1080p80 ISP supports 375 Mpixel/s, it could support 12MP@30fps, 4kp45, or 2x 1080p80
	VPU	Video Decoding ● 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) ● 1080p60 VP9 Profile 0, 2 ● 1080p60 VP8 ● 1080p60 AVC/H.264 Baseline, Main, High decoder Video Encoding ● 1080p60 AVC/H.264 encoder ● 1080p60 HEVC/H.265 encoder
Display Controller	LCDIF	● Total three LCDIF controller, 1-ch HDMI, 1-ch LVDS, 1-ch MIPI DSI ● Support 8-bit/16-bit/18-bit/32-bit color depth ● When using 2-ch, it could support 1080p60 ● When using 3-ch display, it supports 1x1080p60 + 2x720p60 ● The highest resolution is 3840x2160p30
Display	HDMI	● HDMI 2.0a, HDCP 2.2 and HDCP 1.4 encryption technology

Port		● Pixel : 740x480p60, 720x480p60, 1280x720p60, 1920x1080p60 ● Support HDMI 2.1 eARC
	LVDS	● Dual-channel LVDS ● Single channel supports 1366x768p60，PCLK=80MHz ● Dual-channel supports 1366x768P60 to 1080p60,PCLK
	MIPI DSI	● Compliance with MIPI-DSI V1.2 ● Highest resolution: 1080p60,24-bit RGB ● Support biggest channel 4LANE ● HS:80-1.5Gbps/LANE,LP:10Mbps
Video Input	MIPI CSI	● Support 2*4-lane MIPI CSI camera input ● When using 1*ISP, support MIPI CSI 1, PCLK=400MHz (Normal), bandwidth 80-1.5Gbps/lane. ● When using 2*ISP, support MIPI CIS 1&2: PCLK=266MHZ(normal), bandwidth 80-1.5Gbps/LANE, when only using two data LANE, the rate support 1.5Gbps/lane ● Support formats RAW8, RAW10, RAW14, YCbCr420, YCbCR422
Audio		● Audio DSP, working frequency 800MHz ● SPDIF IN &OUT ● 6-ch SAI, support I2S, AC97, TDM ● BCLK=49.152MHz ● 8 kHz to 384kHz sampling rate ● Support audio sampling rate conversion from 1/16 to 8x ● Support 8-ch PDM MIC input
Interface	PCIE	● PCIE3.0*1, XX1-LANE, 8GT/S encoding format 128b/130b, backward compatible with encoding format 8b/10b
	USB	● USB3.0*2, also support USB2.0, bandwidth 5Gbps
	ENET	● RGMII&RMII*2, both support EEE, AVB, IEEE1588, ENET support TSN
	uSDHC	● uSDHC*3 ● uSDHC1&uSDHC3 support EMMC5.1, support HS400 DDR mode, Maximum 400MB/S ● SDIO/SD 3.01 conforms to SDR mode, 200MHZ clock rate is up to 100MB/S ● Support SDXC
	CAN/CANFD	● CAN/CANFD*2
	UART	● UART*4 ● The baud rate of fast mode is up to 4.15 Mbit/s. ● Low-speed mode(IR) baud rate 115.2 Kbit/s ● UART2&A53 DEBUG UART4&M7 DEBUG
	I2C	● I2C*6 ● Standard mode: 100Kbit/S ● Fast mode: 400Kbit/S
	SPI	● SPI*3

2.2. Development Board Resources

SOM Resources	CPU	NXP i.MX8M Plus
	Processor	Quad ARM® Cortex™-A53 core+ Cortex-M7 core, i.MX8M Plus processor's frequency@ 1.6GHz, Cortex®-M7 processor's frequency @800 MHz
	GPU	GC7000UL with OpenCL and Vulkan, support 16 GFLOPS(high precision) OpenGL ES 3.0/3.1, Vulkan, Open CL 1.2FP, OpenVG1.1
	VPU	Support 1080p60, h.265/4, VP8, VP9 video decoding □Support 1080p60, h.265/4 video encoding
	NPU	Neural processor unit: 2.3 TOPS in max.
	RAM	2GB LPDDR4(Std.) (4GB LPDDR4 Optional)
	Flash	16GB eMMC(Std.) (32GB eMMC Optional)
	PMIC	NXP PCA9450 power management unit
	Ethernet	2-ch network chip adopts RGMII mode to perfectly support 10M/100M/1000Mbps Ethernet
	WiFi	Onboard WiFi module, support 2.4GHz/5GHz dual-band WiFi, 802.11a/b/g/n/ac protocol
Carrier Board Resources	Communication	1-ch UART debug port (RS232 level)
		4-ch RS232 serial port (3-wire RS232 UART) 1-ch RS485 port
		2-ch CAN port
		1-ch UART debut port (RS232 level)
	Display	1-ch dual-channel LVDS display interface, resolution up to 1920x1080@60Hz
		1-ch HDMI display interface (HDMI 2.0), resolution up to 4096x2304@60Hz
		1-ch eDP interface, resolution up to 2560x1600@60Hz
	Audio	Audio output_Dual channel stereo Speaker

		Audio output _Single channel stereo HeadPhone
		MIC audio input
	USB	3-ch USB 3.0 Host
		1-ch USB Type-c
	Camera	2-ch MIPI-CSI (4-Lane), support simultaneous input of two cameras, resolution up to 2*1080p@80Hz
	Input	Standard I2C capacitive screen interface
	Extension	M.2 B-KEY interface (USB 3.0), to connect external 4G/ 5G module, SIM card socket
		M.2 M-KEY interface (PCIE3.0), to connect external SSD module
	Storage	1-ch TF Card socket
		1-ch SATA
	Other Devices	Reset circuit, watchdog circuit, real-time clock
	Power Input	+12V DC
SDK	Development Tools	Development environment: virtual machine VM15.5.0+Ubuntu 20.04 or other Linux distribution
		Application developing and debugging tools
		Cross-compiler
		Common terminal developing and debugging tools
	System Image	The matched Image file for the operating system
	Test Program	Demo Interface application demo test program and test program source code
	Source Code	Bootloader, kernel, Bootloader, kernel, file system source code

	Manual	Hardware manual, test manual, device manual, etc
	Schematic	Schematic of the Carrier board (PDF file)
	Mechanical Drawing	Carrier board mechanical drawing (DXF file)
Electricity	Layer/ Size	SOM Size：50mm*82mm,10-layer board high-precision immersion gold process
		Carrier Board Size:140mm*200mm,4-layer board high-precision immersion gold process
	Power Consumption	Power consumption <3W (Non-loaded)
	Operation Temperature	-40℃ ~ +85℃
	Storage Temperature	0℃ ~ +70℃
	Working Humidity	10% to 90%, non-condensing
	SOM Option 1	2GB DDR/16GB eMMC（-40℃ ~ +85℃

2.3.SOM Resources

SMARC-IMX8MP-CM SOM adopts 10-layer PCB board high-precision immersion gold process, high TG board, with reliable electrical performance and anti-interference performance. It integrated with CPU, LPDDR4, eMMC, power management chip, etc. It adopts SMARC 2.1 standard port ,which fully expand the hardware resources of i.MX8MPlus, and can multiplex and combine different interface functions according to the pin conditions to make a bottom board that meets the needs.

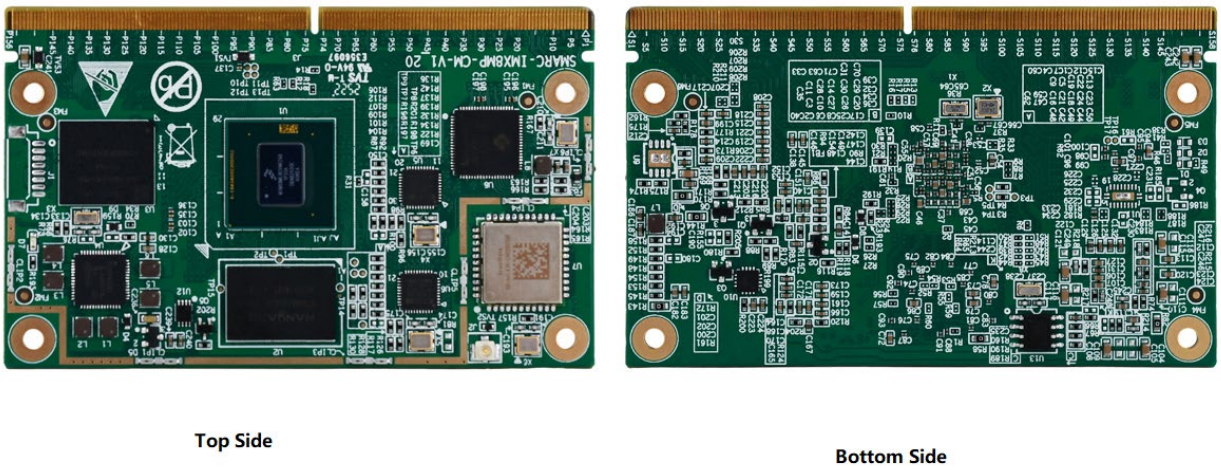

Figure 2

◆Onboard with NXP i.MX8M Plus processor;

◆Onboard with 2GB LPDDR4,16GB eMMc(Standard configuration, industrial grade);

◆The SOM adopts 10-layer PCB board high-precision immersion gold technology;

◆SOM size: 50mm*82mm, it is suitable for various embedded occasions;

◆The SOM adopts standard SMARC port to lead out the SOM resources;

◆Using 5V power supply, onboard power management chip;

◆Onboard with WIFI module;

◆Onboard with 2-ch Ethernet chip

◆Support Linux 6.1 (Yocto), Qt 6.4.2

◆Support Android 11.0

The pin definition of the SOM, please refer to the interface function of carrier board.

Ⅲ.Carrier Board Interface Function

Carrier Board's Block Diagram-Top Side

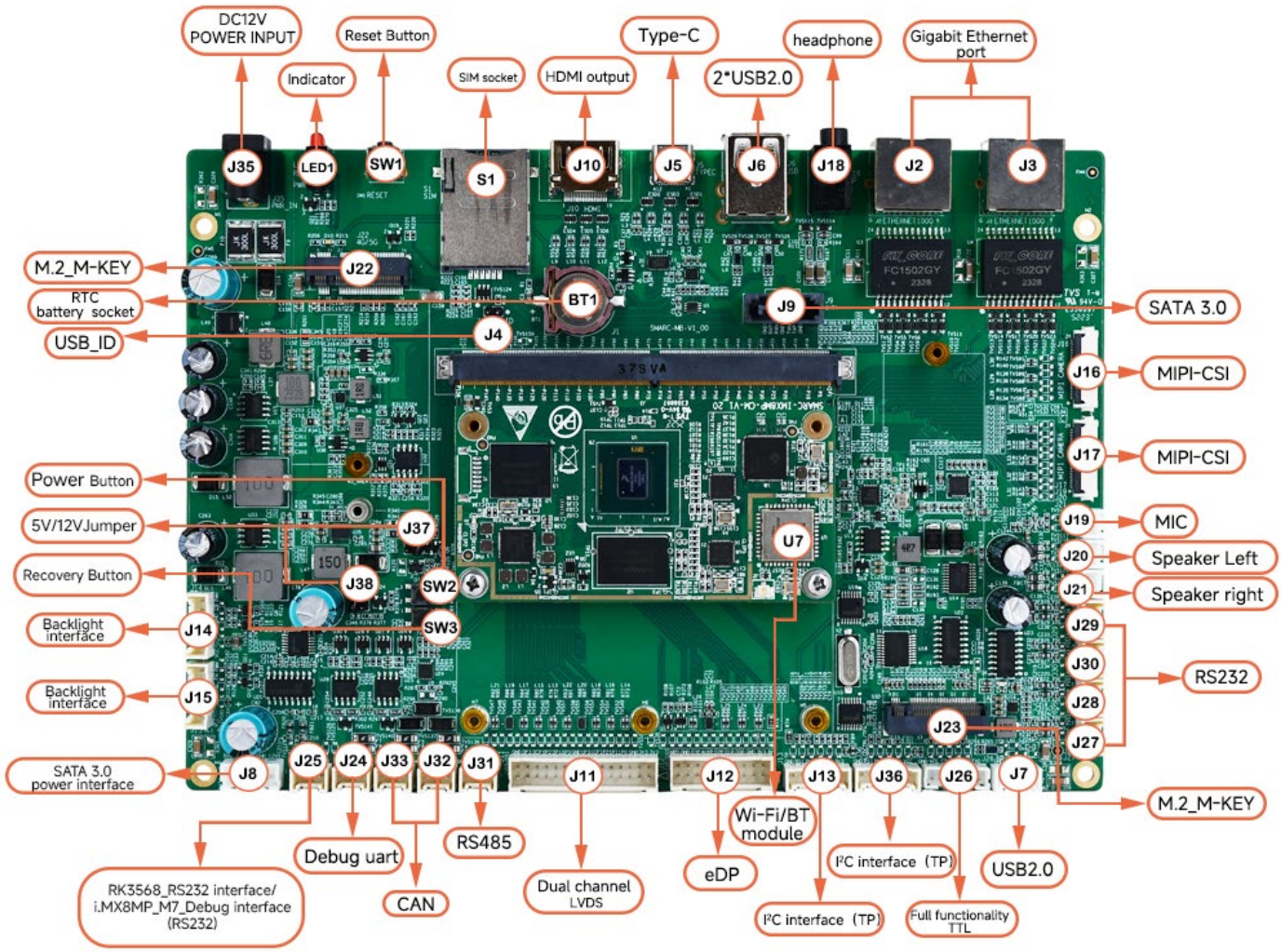

Figure 3

Carrier Board's Block Diagram-Bottom Side

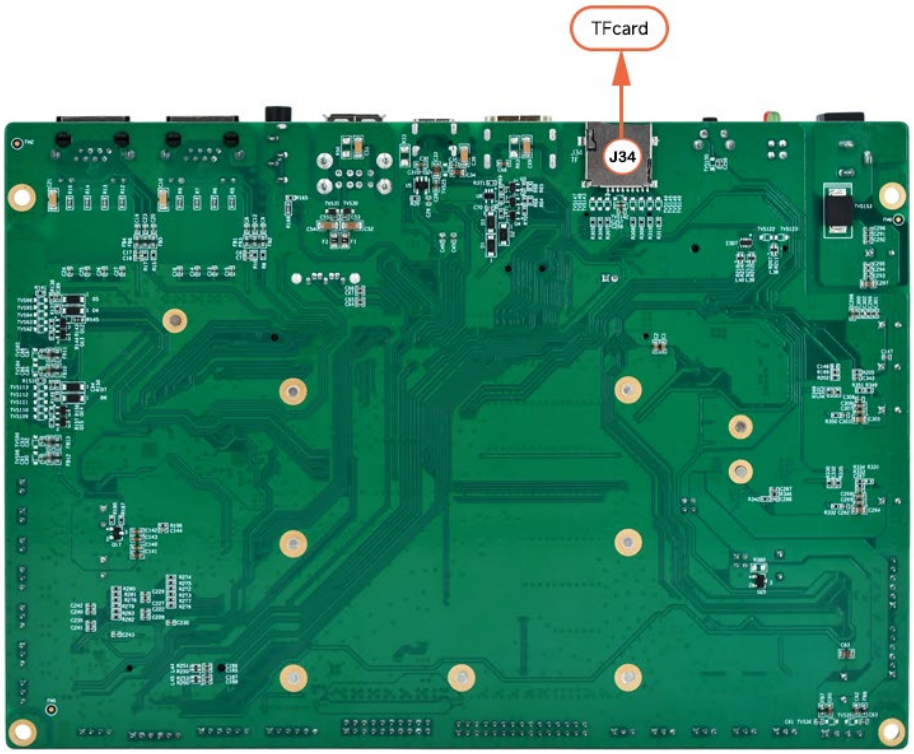

Figure 4

3.1 Interfaces' Functional Description

Label	Functions
J35	DC12V power input interface
LED1	Power Indicator, System Running Indicator
SW1	RESET Button
S1	SIM socket
J10	HDMI output
J5	Type-c

J6	USB2.0 HOST (2*USB2.0)
J18	3.5mm Head Phone Socket
J2	Gigabit Ethernet Interface
J3	Gigabit Ethernet Interface
J9	SATA3.0
J16	MIPI_CSI
J17	MIPI_CSI
J19	MIC
J20	Speak_Left Channel
J21	Speak_Left Channel
J29	RS-232
J30	RS-232
J28	RS-232
J27	RS-232
J23	M.2_M-KEY(PCIE3.0 protocol）
J7	USB2.0
J26	Full functional _ TTL
J36	I2C Port (TP)
J13	I2C Port (TP)
J12	EDP Port
J11	Double Channel LVDS port
J31	RS-485
J32	CAN
J33	CAN
J24	Debug port (RS-232 protocol)
J25	RK3568_RS232\i.MX8MP_M7_Debug port(RS232)
J8	SATA 3.0 power port

J15	Backlight port
J14	Backlight port
SW3	Recovery button
SW4	Power button
BT1	RTC battery socket
J22	M.2_B-KEY (USB3.0 protocol)

3.2.Pin Definition

Pin Definition of SMARC connector through SOM

Pin#	Signal Name	Functional Description	IO	Level
P1	NC			
P2	GND			
P3	MIPI_CSI2_RX_CLK_P	CSI differential signal		Protocol level
P4	MIPI_CSI2_RX_CLK_N			
P5	NC			
P6	NC			
P7	MIPI_CSI2_RX_D0_P	CSI differential signal		Protocol level
P8	MIPI_CSI2_RX_D0_N			
P9	GND			
P10	MIPI_CSI2_RX_D1_P	CSI differential signal		Protocol level
P11	MIPI_CSI2_RX_D1_N			
P12	GND			
P13	MIPI_CSI2_RX_D2_P	CSI differential signal		Protocol level
P14	MIPI_CSI2_RX_D2_N			
P15	GND			
P16	MIPI_CSI2_RX_D3_P	CSI differential signal		Protocol level
P17	MIPI_CSI2_RX_D3_N			
P18	GND			
P19	ENET0_TRX3_N	MDI		Protocol level
P20	ENET0_TRX3_P			
P21	ENET0_LED1	Ethernet Indicator		3.3V
P22	ENET0_LED2			

P23	ENET0_TRX2_N	MDI		Protocol level
P24	ENET0_TRX2_P			
P25	ENET0_LED0	Ethernet Indicator		3.3V
P26	ENET0_TRX1_N	MDI		Protocol level
P27	ENET0_TRX1_P			
P28	NC			
P29	ENET0_TRX0_N	MDI		Protocol level
P30	ENET0_TRX0_P			
P31	NC			
P32	GND			
P33	SD2_WP	SDIO write protection	GPIO2_IO20	3.3V/1.8V
P34	SD2_CMD	SDIO Command	GPIO2_IO14	1.8V/3.3V, default 3.3V
P35	SD2_nCD	SDIO Card Detect	GPIO2_IO12	3.3V/1.8V, pulled-up
P36	SD2_CLK	SDIO Clock	GPIO2_IO13	1.8V/3.3V, default 3.3V
P37	SD2_nRESET	SDIO Reset	GPIO2_IO19	1.8V/3.3V
P38	GND			
P39	SD2_DATA0	SDIO Data	GPIO2_IO15	1.8V/3.3V, default 3.3V
P40	SD2_DATA1		GPIO2_IO16	1.8V/3.3V, default 3.3V
P41	SD2_DATA2		GPIO2_IO17	1.8V/3.3V, default 3.3V
P42	SD2_DATA3		GPIO2_IO18	1.8V/3.3V, default 3.3V
P43	ESPI2_SS0	SPI Chip Select	GPIO5_IO13	1.8V/3.3V, default 1.8V
P44	ESPI2_SCLK	SPI Clock	GPIO5_IO10	1.8V/3.3V, default 1.8V
P45	ESPI2_MISO	SPI MISO	GPIO5_IO12	1.8V/3.3V, default 1.8V

P46	ESPI2_MOSI	SPI MOSI	GPIO5_IO11	1.8V/3.3V, default 1.8V
P47	GND			
P48	NC			
P49	NC			
P50	GND			
P51	NC			
P52	NC			
P53	GND			
P54	QSPI_A_nSS0	SPI Chip Select	GPIO3_IO1	1.8V
P55	NC			
P56	QSPI_A_SCLK	SPI Clock	GPIO3_IO0	1.8V
P57	QSPI_A_DATA1	SPI Data	GPIO3_IO7	1.8V
P58	QSPI_A_DATA0		GPIO3_IO6	1.8V
P59	GND			
P60	USB_DP3_DP	USB2.0		Protocol level
P61	USB_DM3_DM			
P62	USB_DP3_PWREN			3.3V
P63	NC			
P64	NC			
P65	USB_DP2_DP	USB2.0		Protocol level
P66	USB_DM2_DM			
P67	USB_DP2_PWREN			3.3V
P68	GND			
P69	USB_DP1_DP	USB2.0		Protocol level
P70	USB_DM1_DM			

P71	USB_DP1_PWREN			3.3V
P72	NC			
P73	NC			
P74	NC			
P75	PCIE_A_nRST	PCIE3.0 Reset	GPIO4_IO2	3.3V
P76	NC			
P77	NC			
P78	PCIE_A_nCLKREQ	PCIE3.0 Interruption Clock	GPIO4_IO3	3.3V
P79	GND			
P80	NC			
P81	NC			
P82	GND			
P83	PCIE_REF_CLK_P	PCIE 3.0 reference clock input		Protocol level
P84	PCIE_REF_CLK_N			
P85	GND			
P86	PCIE_A_RXP	PCIE3.0 data		Protocol level
P87	PCIE_A_RXN			
P88	GND			
P89	PCIE_A_TXP	PCIE3.0 data		Protocol level
P90	PCIE_A_TXN			
P91	GND			
P92	HDMI_TX2P	HDMI data		Protocol level
P93	HDMI_TX2N			
P94	GND			
P95	HDMI_TX1P	HDMI data		Protocol level

P96	HDMI_TX1N			
P97	GND			
P98	HDMI_TX0P	HDMI data		Protocol level
P99	HDMI_TX0N			
P100	GND			
P101	HDMI_TXCP	HDMI data		Protocol level
P102	HDMI_TXCN			
P103	GND			
P104	HDMI_TX_HPD	HDMI hot-swappable		3.3v/1.8V
P105	HDMI_DDC_SCL	HDMI I2C Bus	GPIO3_IO26	1.8V, pulled-up
P106	HDMI_DDC_SDA		GPIO3_IO27	1.8V, pulled-up
P107	HDMI_CEC	HDMI Control	GPIO3_IO28	1.8V
P108	GPIO_CAM0_nPWR	Camera power, reset_ GPIO	GPIO1_IO00	1.8V/3.3V, default 1.8V
P109	GPIO_CAM1_nPWR		GPIO1_IO01	1.8V/3.3V, default 1.8V
P110	GPIO_CAM0_nRST		GPIO1_IO13	1.8V/3.3V, default 1.8V
P111	GPIO_CAM1_nRST		GPIO1_IO14	1.8V/3.3V, default 1.8V
P112	GPIO4	GPIO	GPIO1_IO05	1.8V/3.3V, default 1.8V
P113	PWM2_OUT	PWM	GPIO1_IO09	1.8V/3.3V, default 1.8V
P114	ESPI1_MISO	SPI MISO	GPIO5_IO8	1.8V/3.3V, default 1.8V
P115	ESPI1_MOSI	SPI MOSI	GPIO5_IO7	1.8V/3.3V, default 1.8V
P116	ESPI1_SCLK	SPI Clock	GPIO5_IO6	1.8V/3.3V, default 1.8V
P117	ESSPI1_SS0	SPI Chip Select	GPIO5_IO9	1.8V/3.3V, default 1.8V

P118	GPIO10	GPIO	GPIO5_IO3	1.8V/3.3V, default 1.8V
P119	GPIO11	GPIO	GPIO5_IO4	1.8V/3.3V, default 1.8V
P120	GND			
P121	NC			
P122	NC			
P123	BOOT_MODE0	Boot mode switch		1.8V/3.3V
P124	BOOT_MODE1			1.8V/3.3V
P125	NC			
P126	GPIO_nRST_OUT	GPIO reset out	GPIO4_IO24	1.8V/3.3V, default 1.8V
P127	PMIC_nRST	Power management chip reset		3.3V, pulled-up
P128	NC			
P129	I/F_UART_TXD	UART	GPIO2_IO8	1.8V/3.3V, default 1.8V
P130	I/F_UART_RXD		GPIO2_IO9	
P131	I/F_UART_CTSn	UART flow control	GPIO2_IO11	
P132	I/F_UART_RTSn		GPIO2_IO10	
P133	GND			
P134	UART4_TXD	UART	GPIO5_IO29	1.8V/3.3V, default 1.8V
P135	UART4_RXD		GPIO5_IO28	
P136	UART1_TXD	UART	GPIO5_IO23	1.8V/3.3V, default 1.8V
P137	UART1_RXD		GPIO5_IO22	
P138	UART1_CTS_B		GPIO5_IO26	1.8V/3.3V, default 1.8V
P139	UART1_RTS_B		GPIO5_IO27	
P140	UART2_TXD	UART	GPIO5_IO25	1.8V/3.3V, default 1.8V
P141	UART2_RXD		GPIO5_IO24	

P142	GND			
P143	CAN1_TXD	CAN	GPIO4_IO22	1.8V/3.3V, default 1.8V
P144	CAN1_RXD		GPIO4_IO25	
P145	CAN2_TXD	CAN	GPIO4_IO26	1.8V/3.3V, default 1.8V
P146	CAN2_RXD		GPIO4_IO27	
P147	5V0	SOM 5V power input		
P148	5V0			
P149	5V0			
P150	5V0			
P151	5V0			
P152	5V0			
P153	5V0			
P154	5V0			
P155	5V0			
P156	5V0			
S1	I2C3_SCL	I2C	GPIO5_IO18	1.8V, pulled-up
S2	I2C3_SDA		GPIO5_IO19	
S3	GND			
S4	NC			
S5	I2C4_SCL	I2C	GPIO5_IO20	1.8V, pulled-up
S6	CCM_CLKO2	Main clock output	GPIO1_IO15	1.8V
S7	I2C4_SDA	I2C	GPIO5_IO21	1.8V, pulled-up
S8	MIPI_CSI1_CLK_P	CSI differential clock		Protocol level
S9	MIPI_CSI1_CLK_N			
S10	GND			

S11	MIPI_CSI1_D0_P	CSI differential		Protocol level
S12	MIPI_CSI1_D0_N			
S13	GND			
S14	MIPI_CSI1_D1_P	CSI differential input		Protocol level
S15	MIPI_CSI1_D1_N			
S16	GND			
S17	ENET1_TRX0_P	MDI		Protocol level
S18	ENET1_TRX0_N			
S19	ENET1_LED1	Ethernet Indicator		3.3V, pulled-up
S20	ENET1_TRX1_P	MDI		Protocol level
S21	ENET1_TRX1_N			
S22	ENET1_LED2	Ethernet Indicator		3.3V, pulled-up
S23	ENET1_TRX2_P	MDI		Protocol level
S24	ENET1_TRX2_N			
S25	GND			
S26	ENET1_TRX3_P	MDI		Protocol level
S27	ENET1_TRX3_N			
S28	NC			
S29	NC			
S30	NC			
S31	ENET1_LED0	Ethernet Indicator		3.3V, pulled-up
S32	NC			
S33	NC			
S34	GND			
S35	NC			

S36	NC			
S37	USB1_VBUS	USB3.0 Device Insert detection		5V
S38	SAI5_MCLK	SAI Audio	GPIO3_IO25	1.8V
S39	SAI5_TXFS		GPIO3_IO22	
S40	SAI5_TXD0		GPIO3_IO24	
S41	SAI5_RXD0		GPIO3_IO21	
S42	SAI5_TXC		GPIO3_IO23	
S43	NC			
S44	NC			
S45	NC			
S46	NC			
S47	GND			
S48	I2C3_SCL	I2C Bus	GPIO5_IO18	1.8V/3.3V, default 1.8V, pulled-up
S49	I2C3_SDA		GPIO5_IO19	
S50	NC			
S51	NC			
S52	NC			
S53	NC			
S54	NC			
S55	USB_DP4_PWREN	USB power		3.3V
S56	QSPI_A_DATA2	SPI data	GPIO3_IO8	1.8V
S57	QSPI_A_DATA3		GPIO3_IO9	1.8V
S58	NC			
S59	USB_DP4_DP			
S60	USB_DP4_DM			

S61	GND			
S62	USB1_TX_P	USB3.0		Protocol level
S63	USB1_TX_N			
S64	GND			
S65	USB1_RX_P	USB3.0		Protocol level
S66	USB1_TX_N			
S67	GND			
S68	USB1_D_P	USB3.0		Protocol level
S69	USB1_D_N			
S70	GND			
S71	USB1_DP1_SSTXP	USB3.0		Protocol level
S72	USB1_DP1_SSTXN			
S73	GND			
S74	USB1_DP1_SSRXP	USB3.0		Protocol level
S75	USB1_DP1_SSRXN			
S76	NC			
S77	NC			
S78	NC	PCIE2.0 data		Protocol level
S79	NC			
S80	GND			
S81	NC	PCIE2.0 data		Protocol level
S82	NC			
S83	GND			
S84	NC			
S85	NC			

S86	GND			
S87	PCIE_B_RXP	PCIE3.0 data		Protocol level
S88	PCIE_B_RXN			
S89	GND			
S90	PCIE_B_TXP	PCIE3.0 data		Protocol level
S91	PCIE_B_TXN			
S92	GND			
S93	MIPI_DSI_D0_P	MIPI Display Data		Protocol level
S94	MIPI_DSI_D0_N			
S95	NC			
S96	MIPI_DSI_D1_P	MIPI Display Data		Protocol level
S97	MIPI_DSI_D1_N			
S98	NC			
S99	MIPI_DSI_D2_P			Protocol level
S100	MIPI_DSI_D2_N			
S101	GND			
S102	MIPI_DSI_D3_P	MIPI Display Data		Protocol level
S103	MIPI_DSI_D3_N			
S104	USB1_ID	USB3.0 OTG ID		3.3V
S105	MIPI_DSI_CLK_P	MIPI Display Clock		Protocol level
S106	MIPI_DSI_CLK_N			
S107	GPIO_LCD1_BKLT_EN	LCD backlight enable GPIO	GPIO1_IO07	1.8V/3.3V, default 1.8V
S108	LVDS1_CLK_P	LVDS clock		Protocol level
S109	LVDS1_CLK_N			
S110	GND			

S111	LVDS1_D0_P	LVDS data		Protocol level
S112	LVDS1_D0_N			
S113	NC			
S114	LVDS1_D1_P	LVDS data		Protocol level
S115	LVDS1_D1_N			
S116	GPIO_LCD1_VDD_EN	LCD power enable GPIO	GPIO1_IO06	1.8V/3.3V, default 1.8V
S117	LVDS1_D2_P	DSI Differential		Protocol level
S118	LVDS1_D2_N			
S119	GND			
S120	LVDS1_D3_P	DSI Differential		Protocol level
S121	LVDS1_D3_N			
S122	LCD1_BKLT_PWM	LCD backlight PWM	GPIO1_IO08	1.8V/3.3V, default 1.8V
S123	GPIO13	GPIO	GPIO5_IO5	1.8V/3.3V, default 1.8V
S124	GND			
S125	LVDS0_D0_P	LVDS data		Protocol level
S126	LVDS0_D0_N			
S127	GPIO_LCD0_BKLT_EN		GPIO1_IO12	1.8V/3.3V, default 1.8V
S128	LVDS0_D1_P			Protocol level
S129	LVDS0_D1_N			
S130	GND			
S131	LVDS0_D2_P	DSI And LVDS multiplexed		Protocol level
S132	LVDS0_D2_N			
S133	GPIO_LCD0_VDD_EN	LCD power enable GPIO	GPIO1_IO11	1.8V/3.3V, default 1.8V
S134	LVDS0_CLK_P	DSI And LVDS multiplexed		Protocol level
S135	LVDS0_CLK_N			

S136	GND			
S137	LVDS0_D3_P	DSI And LVDS multiplexed		Protocol level
S138	LVDS0_D3_N			
S139	I2C2_SCL	I2C bus	GPIO5_IO16	1.8V/3.3V, default 1.8V, pulled-up
S140	I2C2_SDA		GPIO5_IO17	
S141	LCD0_BKLT_PWM	LCD backlight PWM	GPIO1_IO10	1.8V/3.3V, default 1.8V
S142	NC			
S143	GND			
S144	NC			
S145	NC			
S146	PCIE_nWAKE	PCIE3.0 wake	GPIO4_IO20	3.3V
S147	VCC_RTC_3V0			
S148	NC			
S149	GPIO_SLEEP	Sleep GPIO	GPIO4_IO21	1.8V/3.3V, default 1.8V
S150	GPIO_PWR_BAD			
S151	NC			
S152	NC			
S153	GPIO_CARR_nSTBY	GPIO Output	GPIO3_IO19	1.8V
S154	GPIO_CARR_PWRON	GPIO Output	GPIO3_IO20	1.8V
S155	CPU_ONOFF			1.8V
S156	NC			
S157	NC			
S158	GND			

J16: MIPI_CSI

PIN#	Signal Name

1	VCC_CAM0_5V0
2	GND
3	VCC_CAM0_3V3
4	VCC_CAM0_3V3
5	GND
6	CSI0_CK_N
7	CSI0_CK_P
8	GND
9	CSI0_RX0_N
10	CSI0_RX0_P
11	GND
12	CSI0_RX1_N
13	CSI0_RX1_P
14	GND
15	NC
16	NC
17	GND
18	NC
19	NC
20	GND
21	CSI0_I2C_SDA
22	CSI0_I2C_SCL
23	CSI0_PWDN
24	CSI0_nRST
25	GND

26	CSI0_PWR_EN

J17: MIPI_CSI

PIN#	Signal Name
1	VCC_CAM1_5V0
2	GND
3	VCC_CAM1_3V3
4	VCC_CAM1_3V3
5	GND
6	CSI1_CK_N
7	CSI1_CK_P
8	GND
9	CSI1_RX0_N
10	CSI1_RX0_P
11	GND
12	CSI1_RX1_N
13	CSI1_RX1_P
14	GND
15	NC
16	NC
17	GND
18	NC
19	NC
20	GND
21	CSI1_I2C_SDA
22	CSI1_I2C_SCL

23	CSI1_PWDN
24	CSI1_nRST
25	GND
26	CSI1_PWR_EN

J19: MIC

PIN#	Signal Name
1	AUD_MIC+
2	AUD_MIC-

J20: Speak_Left

PIN#	Signal Name
1	AUD_AMP_OUTPL
2	AUD_AMP_OUTNL

J21: Speak_Right

PIN#	Signal Name
1	AUD_AMP_OUTPR
2	AUD_AMP_OUTNR

J29/J30/J28/J27: RS-232

PIN#	Signal Name
1	COM_TX
2	COM_RX
3	GND

J7:USB2.0

PIN#	Signal Name
1	VCC_EXT_5V0

2	USB5_DN_CON
3	USB5_DP_CON
4	GND

J26:Full function_ TTL

PIN#	Signal Name
1	TXD_TTL
2	RXD_TTL
3	RTS_TTL
4	CTS_TTL
5	VCC_IO
6	GND

J23: M.2_M-KEY(PCIE3.0）

Signal Name	PIN#	PIN#	Signal Name
GND	1	2	VCC_SSD_3V3
GND	3	4	VCC_SSD_3V3
NC	5	6	NC
NC	7	8	NC
GND	9	10	LED
NC	11	12	VCC_SSD_3V3
NC	13	14	VCC_SSD_3V3
GND	15	16	VCC_SSD_3V3
NC	17	18	VCC_SSD_3V3
NC	19	20	NC
GND	21	22	NC
NC	23	24	NC

NC	25	26	NC
GND	27	28	NC
NC	29	30	NC
NC	31	32	NC
GND	33	34	NC
NC	35	36	NC
NC	37	38	NC
GND	39	40	VCC_SSD_3V3
SSD_PET0_N	41	42	VCC_SSD_3V3
SSD_PET0_P	43	44	NC
GND	45	46	NC
SSD_PER0_N	47	48	NC
SSD_PER0_P	49	50	PCIE_A_nRST
GND	51	52	PCIE_A_nCKREQ
SSD_REFCLK_N	53	54	PCIE_nWAKE
SSD_REFCLK_P	55	56	NC
GND	57	58	NC
STD M-KEY	• • •	• • •	STD M-KEY
NC	67	68	NC
NC	69	70	VCC_SSD_3V3
GND	71	72	VCC_SSD_3V3
GND	73	74	VCC_SSD_3V3
GND	75		

J36: I2C(TP)

PIN#	Signal Name

1	VCC_IO
2	I2C2_SCL
3	I2C2_SDA
4	GPIO_LCD0_nINT
5	GPIO_LCD0_nRST
6	GND

J13: I2C(TP)

PIN#	Signal Name
1	VCC_EXT_3V3
2	TP_I2C_SCL
3	TP_I2C_SDA
4	TP_nINT
5	TP_nRST
6	GND

J12: EDP

Signal Name	PIN#	PIN#	Signal Name
VCC_LCD_5V0	1	2	VCC_LCD_3V3
VCC_LCD_5V0	3	4	VCC_LCD_3V3
GND	5	6	GND
LCD2_D0_N	7	8	LCD2_D0_P
LCD2_D1_N	9	10	LCD2_D1_P
LCD2_D2_N	11	12	LCD2_D2_P
LCD2_AUX_N	13	14	LCD2_AUX_P
LCD2_D3_N	15	16	LCD2_D3_P
GND	17	18	GND

LCD2_nRST	19	20	LCD2_HPD

J11: Dual-channel LVDS

Signal Name	PIN#	PIN#	Signal Name
VCC_LCD_5V0	1	2	VCC_LCD_3V3
VCC_LCD_5V0	3	4	VCC_LCD_3V3
GND	5	6	GND
LCD1_D0_N	7	8	LCD1_D0_P
LCD1_D1_N	9	10	LCD1_D1_P
LCD1_D2_N	11	12	LCD1_D2_P
LCD1_CK_N	13	14	LCD1_CK_P
LCD1_D3_N	15	16	LCD1_D3_P
GND	17	18	GND
LCD0_D0_N	19	20	LCD0_D0_P
LCD0_D1_N	21	22	LCD0_D1_P
LCD0_D2_N	23	24	LCD0_D2_P
LCD0_CK_N	25	26	LCD0_CK_P
LCD0_D3_N	27	28	LCD0_D3_P
GND	29	30	GND

J31：RS-485

PIN#	Signal Name
1	RS485_A
2	RS485_B
3	GND

J32/J33：CAN

PIN#	Signal Name
1	CAN_H
2	CAN_L
3	GND

J24: DebugUART (RS-232 protocol)

PIN#	Signal Name
1	COM_TXD
2	COM_RXD
3	GND

J25:Rk3568_RS232 INTERFACE\i.MX8MP_M7_Debug Interface (RS232)

PIN#	Signal Name
1	COM_TXD
2	COM_RXD
3	GND

J8: SATA3.0 power

PIN#	Signal Name
1	VCC_SATA_12V0
2	GND
3	GND
4	VCC_SATA_5V0

J15/J14:Backlight

PIN#	Signal Name
1	VCC_BL
2	VCC_BL

3	GND
4	GND
5	BL0_EN
6	BL0_PWM

J22:M.2_B-KEY (USB3.0 protocol)

Signal Name	PIN#	PIN#	Signal Name
GND	1	2	VCC_5G_3V8
GND	3	4	VCC_5G_3V8
GND	5	6	5G_ON_OFF
5G_USB_D_P	7	8	5G_DISEN
5G_USB_D_N	9	10	5G_STATE
GND	11	…	STD B-KEY
STD B-KEY	…	20	NC
GND	21	22	NC
NC	23	24	NC
NC	25	26	NC
GND	27	28	NC
5G_USB_SSRX_N	29	30	USIM_nRST
5G_USB_SSRX_P	31	32	USIM_CLK
GND	33	34	USIM_DATA
5G_USB_SSTX_N	35	36	USIM_VDD
5G_USB_SSTX_P	37	38	VCC_EXT_1V8
GND	39	40	NC
NC	41	42	NC
NC	43	44	NC

GND	45	46	NC
NC	47	48	NC
NC	49	50	VCC_EXT_3V3
GND	51	52	VCC_EXT_3V3
NC	53	54	VCC_EXT_3V3
NC	55	56	NC
GND	57	58	NC
NC	59	60	NC
NC	61	62	NC
NC	63	64	NC
NC	65	66	NC
5G_nRST	67	68	NC
GND	69	70	VCC_5G_3V8
GND	71	72	VCC_5G_3V8
GND	73	74	VCC_5G_3V8
NC	75		

Ⅳ.Structural Drawing

Unit: mm, please email us for the size of the connector:supports@qiyangtech.com；

4.1.SOM Dimension

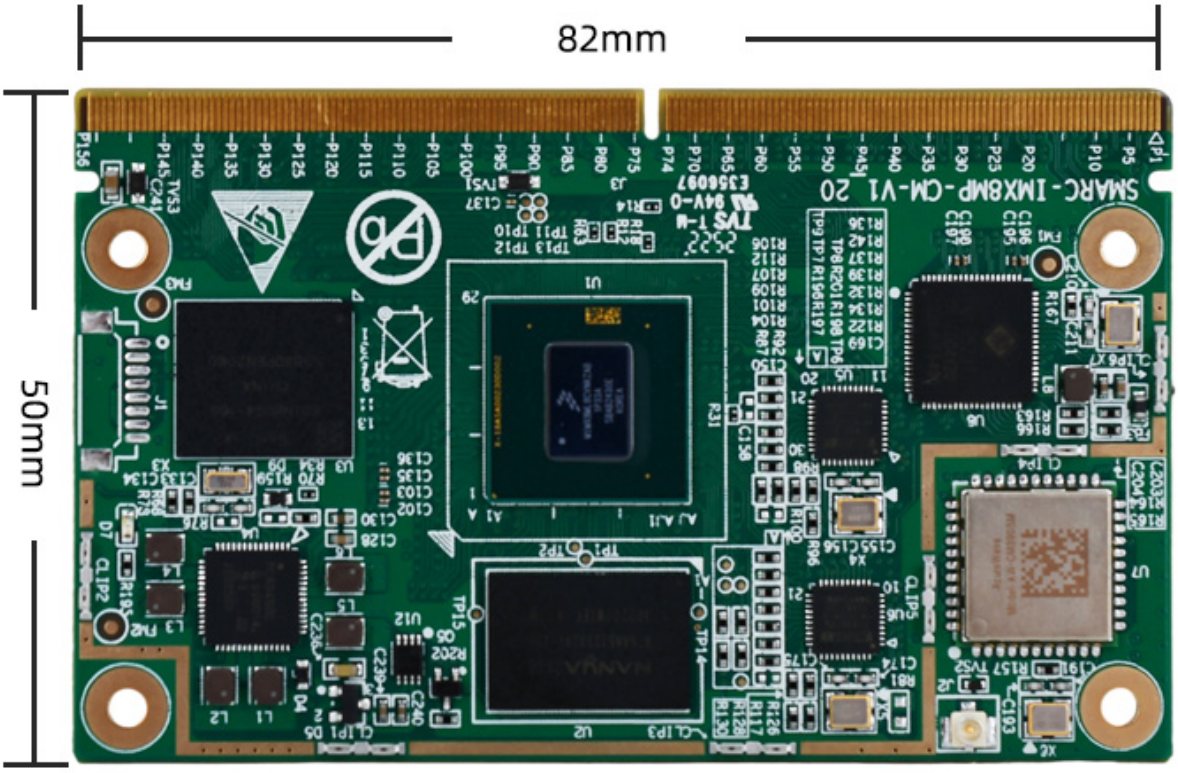

Figure 5

4.2.Carrier Board Dimension

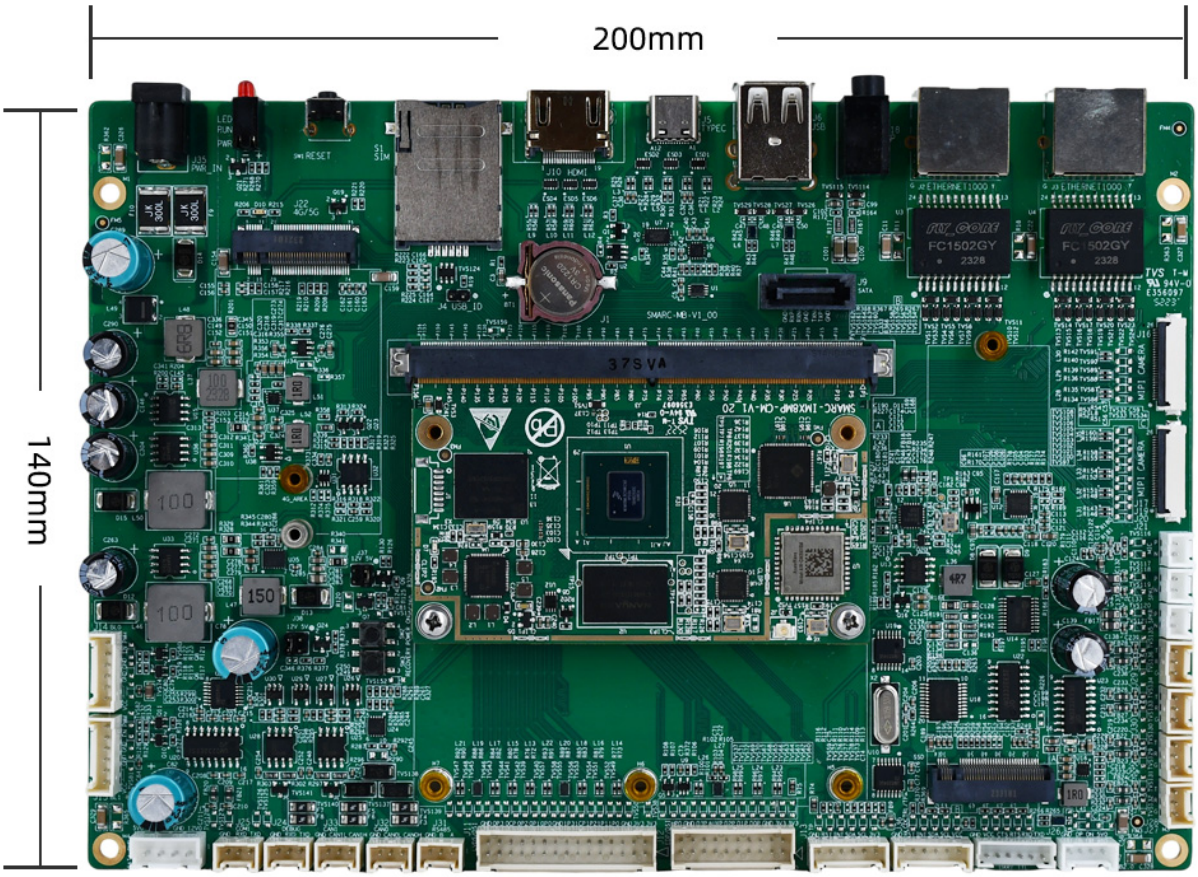

Figure 6

V. Connection Diagram

Pay attention to the orientation of the SOM: (Refer to the figure below)

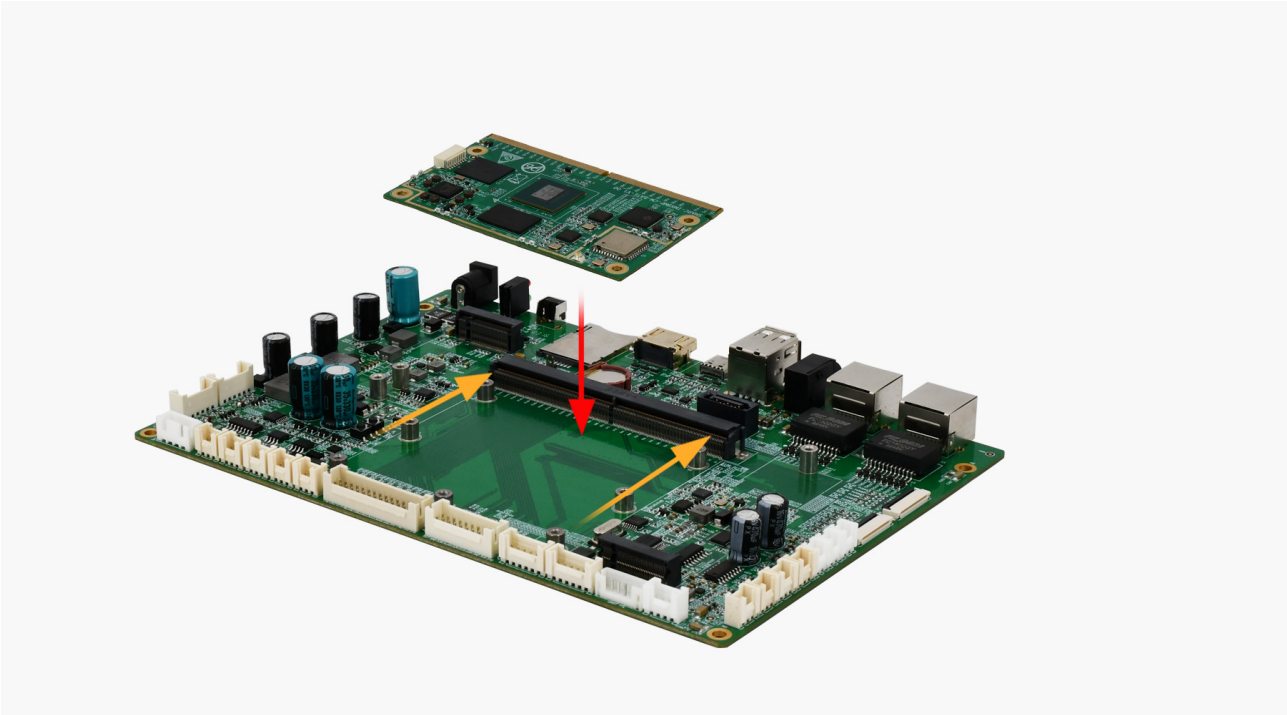

Figure 7

Ⅵ. Electrical Specification

Item	Parameters
Operating Temperature	-40℃ ~ +85℃
Storage Temperature	0℃ ~ +70℃
Operating Humidity	5%~95%，Non-Condensing
SOM Size	50mm*82mm,10-layer high precision gold immersion process
Carrier Board Size	140mm*200mm,4-layer high precision gold immersion process
Whole Board Power Consumption	＜5W（Non-Loaded）
Power Supply	DC12V/2A

Ⅶ. Software Description

SMARC-IMX8MP-KIT mainly supports Linux /Android.

The ***SMARC-IMX8MP-KIT Linux User Manual*** describes in detail the establishment and use of the Linux development environment provided by the SMARC-IMX8MP-KIT development board. For more details, please refer to the related documents.

The ***SMARC-IMX8MP-KIT Android User Manual*** describes in detail the establishment and use of the Android development environment provided by the SMARC-IMX8MP-KIT development board.

For more details, please refer to the relevant documents.

Ⅷ. Remark

1. Before connecting to LCD, please confirm LCD power specification.

2. Please use the original connecting accessories to avoid damaging the main board.

3. We ensure offering communication technology support through E-mail, telephone for lifelong technical support service.

4. We ensure offering 6-months repair service for free, if malfunction occurs in warranty because of quality problem. Under that circumstance, please contact our retailer or our company with purchase receipt within warranty period, we are willing to repair or replace.

5. Under these circumstances, we do not offer repair for free:

● Over warranty time;

● Do not attach purchase receipt;

● Liquid inlet, damp or mold;

● Malfunction and damage is not due to product quality but drops, intense sharking, arbitrarily modify, disoperation after purchase;

● Damage of force majeure.

6. We reserve intellectual property for the software and hardware technical data of SMARC-IMX8MP-KIT; users can only use them for teaching, testing, researching. Shall not be engaged in any commercial purpose. Shall not distribute them on the Internet. Shall not intercept, modify them to tamper copyright.

7. We accept batch order. We can offer technical support and service.

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