SMARC-RK3568-Kit

Hardware Manual

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Information updates

1. Information updates

Product-related manuals and datasheets are constantly being improved and updated; please ensure that they are up-to-date when you use them.

2.Update notice

Qiyang's newest product information and news updates will be released through the WeChat official account, please pay attention!

3.How to get information

After purchase, please contact the relevant sales staff to obtain the SDK.

Version Record

Version	Hardware Platform	Description	Date
1.0	SMARC-RK3568-MB	First version	

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Notice: This manual introduces the hardware interface of the SMARC-RK3568-Kit Development Kit.

Ⅰ. Preface

1.1. Company Profile

Zhejiang Qiyang Intelligent Technology Co., Ltd., established in 2007, which locates in Hangzhou, Zhejiang, PRC. It is a high-end technological enterprise that specializes in exploitation, fabrication, and selling embedded computer mainboards . With 10 years of experiences, Qiyang has established the completed service chain from the design concept to mass production successfully.

The R&D team is organized by 30 more technical engineers. Qiyang focus on providing functional embedded hardware, software tool and customization solutions. It has been applied to Industrial Control, Internet of Things, New Retail, Smart Medical, Electricity Device, Environmental Surveillance, Charging Pile etc.

With the growth of the business, Qiyang has set up an SMT factory in Zhuji, Zhejiang province, which is 5000 ㎡, with a 2xSMT production line. The SMT factory performs the ISO9001 Quality Management System strictly. Relying on the solid production ability, the SMT factory's annual capacity is about a million sets, which totally guarantee the delivery date.

Qiyang has a thorough sales marketing network, professional sales ,and after-sales team to provide full technical support and service. The business has spread over 120 countries and areas, it helps the clients to introduce the products into the market efficiently and successfully.The combination and extension of research and development, production capacity, and market, that provide a solid foundation for Qiyang to provide specialized, globalized embedded hardware and software.

We offer:

l.Software/Hardware Mainboard

Based on the CPU solution from NXP,Rockchip,MTK,Renesas,TI,Atmel,Cirrus Logic etc, Qiyang provides the ARM development kit/system on module/industrial board and periphery products, paired tools and software for the user do further exploitation.

2.Customization Service

Fully taking the advantage of the technical accumulation on the ARM platform and Linux, Android, Ubuntu OS, Qiyang provides the efficient OEM/ODM service to the users.

Sincerely thanks for using Qiyang's product, we will try our best to offer you the technical supports!

1.2. SMARC-RK3568-KIT Development Kit Use Suggestion:

1. Please read the instructions firstly, before using the SMARC-RK3568-Kit development Kit.

2. Before using, please check the packing list and see whether there is a missing file in the CD;

3. Please understand the basic structure and composition of SMARC-RK3568-CM SOM, including the hardware resource allocation etc.;

4. If you need to develop on Debian Linux system and burn program into the development board, in addition, we also suggest reading another documentation ***SMARC-RK3568-Kit Debian Linux User Manual;***

5. If you need to develop on Android system and burn program into the development board, in addition, we also suggest reading another documentation ***SMARC-RK3568-Kit Android User Manual;***

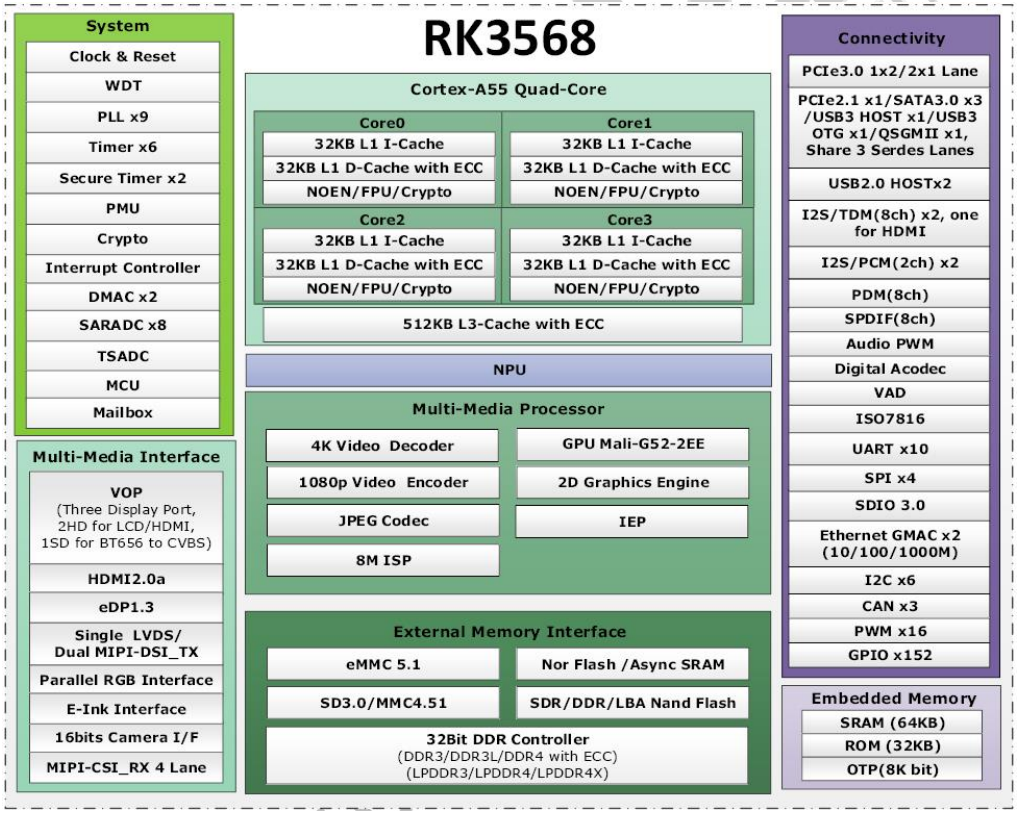
Ⅱ. Introduction

2.1. Overview

RK3568 is a high-performance and low power quad-core application processor designed for personal mobile internet device and AIoT equipments.

Many embedded powerful hardware engines are provided to optimize performance for high end application. RK3568 supports almost full-format H.264 decoder by 4K@60fps, H.265 decoder by 4K@60fps, also support H.264/H.265 encoder by 1080p@60fps, high-quality JPEG encoder/decoder.

Embedded 3D GPU makes RK3568 completely compatible with OpenGL ES 1.1/2.0/3.2, OpenCL 2.0 and Vulkan 1.1. Special 2D hardware engine will maximize display performance and provide very smoothly operation. The build-in NPU supports INT8/INT16/FP16/BFP16 hybrid operation. In addition, with its strong compatibility, network models based on a series of frameworks such as TensorFlow/MXNet/PyTorch/Caffe can be easily converted. RK3568 has high-performance external memory interface(DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X) capable of sustaining demanding memory bandwidths.



Pic 1

Detailed Parameters of CPU:

CORE	CPU	● Quad-core Arm®Cortex®-A55 2.0GHz ● 32 KB Level 1 instruction cache, 32 KB Level 1 data cache and checksum ● 512 KB same standard Level 3 cache and checksum ● Supports 64bit Armv8 architecture
	MCU	● 32bits microprocessor ● Harvard architecture independent instruction and data memory ● Integrated Programmable Interrupt Controller (IPIC) ● Integrated Debug Controller (DEBUG) and JTAG interface
Storage	On-chip storage	● Boot ROM(32KB)---Bootstrap read-only memory（32KB） ● On-chip SRAM SYSTEM(64KB) + PMU(8KB) --- On-chip static random memory (System 64KB + Power Management Unit 8KB)
	External Storage	● 16/32-bit DRAM interface:LPDDR4/4X,LPDDR3,DDR4,DDR3,DDR3L ● 8-bit Asynchronous/ONFI Synchronous NAND FLASH, Toggle Flash，SLC/MLC/TLC Flash，Hardware ECC ● EMMC 5.1 FLASH(support HS200) Compatible 4.41、4.51、5.0Specification，support 1/4/8bit Data Width ● SD3.0/MMC 4.51，4bit Data Width；SPI FLASH support 1/4/8bit Data Width ● FlexSPI Flash， Serial NOR/Nand Flash，support SDR
On-chip unit	GPU	● Mali-G52 1-Core-2EE ● Support OpenGL ES 1.1, 2.0, and 3.2；Vulkan 1.0 and 1.1；OpenCL 2.0 Full Profile；1600Mpix/s（Megapixels/sec）fill rate when 800MHz clock frequency ● Support 38.4GLOPs（Number of floating point operations） when 800MHz clock frequency
	NPU	● 0.8 TOPS(Trillion times per second)，support INT8/INT16Hybrid operation, Deep Learning Architecture.
	ISP	● Support video data from DVP or MIPI CSI---DVP or MIPI CSI Get video data ● Maximum resolution is 4096x2304---Maximum Resolution 4096x2304
	VPU	Video Decoding (Video Decoder) ● H.265 HEVC/MVC Main10 Profile yuv420@L5.1 up to 4096x2304@60fps ● VP9 Profile0/2 yuv420@L5.1 up to 4096x2304@60fps ； ● VP8 verision2,up to 1920x1088@60fps； ● VC1 Simple Profile@low, medium, high levels, Main Profile@low, medium, high levels, Advanced Profile@level0~3,up to 1920x1088@60fps ● MPEG-4 Simple Profile@L0~6,Advanced Simple Profile@L0~5,up to 1920x1088@ 60fps ● MPEG-1/2 Main Profile, low, medium and high levels, up to 1920x1088@60fps

		● H.264 AVC/MVC Main10 Profile yuv400/yuv420/yuv422/@L5.1 up to 4096x2304@ 60fps ● H.263 Profile0,levels 10-70,up to 720x576@60fps Video Decoding (Video Encoder) ● H.264/AVC BP/MP/HP@level4.2，up to 1920x1080@100fps ● H.265/HEVC MP@level4.1, up to 1920x1080@100fps (4096x4096@10fps with TILE) Support YUV/RGB video source rotation and mirroring
Display Controller	VOP	● Video Input：support 2 cluster layer、2 esmart layer and 2 smart layer,4096X2160 Resolution input，RGB/YUV/YUYV Format，Up and down 4~1/4 scale scaling, rotation, 4 regions ● Overlay （Video Overlay）：Supports up to 6 levels 2 Cluster/2 Esmart/2 Smart,Support RGB/YUV overlay ● POST process（Post-processing）:HDR10/HDR HLG，HDR2SDR/SDR2HDR；3D–LUT/P2 I/CSC/BCSH/DITHER/CABC/GAMMA/COLORBAR ● Write back(Writing Board)：ARGB8888/RGB888/RGB565/YUV420 Format；Maximum Resolution 1920X1080 ● Video Output：Video output 0, up to 4096x2304 @ 60Hz resolution; video output 1, up to 2048x1536 @ 60Hz resolution; video output 2, up to 1920x1080 @ 60Hz resolution
Display Interface	HDMI	● Supports HDMI 1.4 and HDMI 2.0 operation all the way to the physical layer PHY ● Up to 10-bit depth color mode; up to 1080p@120Hz and 4096x2304@60Hz resolution; support for 3D video formats; support for HDCP (High-bandwidth Digital Content Protection) 1.4/2.2 protocol ● Supports RGB/YUV (up to 10-bit) format
	LVDS	● Compliant with TIA/EIA-644-A LVDS specification ● LVDS interface supports RGB888 and RGB666 inputs ● Supports VESA/JEIDA LVDS data format transmission
	MIPI DSI	● Compatible with MIPI Alliance Interface Specification V1.2 ● Support dual-channel DSI, each channel supports 4 data lanes ● Each lane supports up to 2.5Gbps rate ● Single MIPI mode: up to 1920x1080@60Hz resolution output; Dual MIPI mode: up to 2560x1440@60Hz resolution output ● Supports RGB (up to 8-bit) format
	eDP	● Supports 1 eDP 1.3 interface, up to 4 physical lanes, 2.7Gbps per lane, up to 2560x1600@60Hz ● Support Panel Self-Refresh (PSR) ● Supports RGB (up to 10-bit) format
	EBC	● Compatible with e-ink screen ● Supports 2200x1650 resolution with 16-bit data lines

		● Up to 16 levels of grayscale and 256 frames per scan
	RGB/BT.1120	● Supports up to 1920x1080@60Hz resolution and RGB (up to 8-bit) format; up to 150MHz data rate
	BT.656	● Support PAL and NTSC
Video input interface	MIPI CSI	● Compatible with MIPI Alliance Interface Specification V1.2 ● Up to 4 data lanes, each lane supports up to 2.5Gbps rate ● Support MIPI high-speed mode (MIPI-HS), MIPI low-power mode (MIPI-LP) ● Support two combinations: ① 1 way clock lane and 4 way data lane; ② 2 way data lane with each clock lane
	DVP	● Supports 8-bit/10-bit/12-bit/16-bit input; up to 150MHz data rate input
	VICAP	● Support BT601 YCbCr 422 8-bit input, RAW 8/10/12-bit input, BT656 YCbCr 422 8-bit input, BT1120 YCbCr 422 8/10/12/16-bit input, single/dual edge sampling; 2/4 mixed BT656/BT1120 YCbCr 422 8-bit input; YUYV sequence configuration; support polarized pixel_clk, hsync and vsync configuration; support CSI2 data protocol (up to 4 IDs) reception, DSI data protocol (video mode/command mode) reception; window cropping support; virtual step support when writing to DDR; YUV data support NV16/NV12 output; raw data compression/uncompressed output support
	ISP	● DVP input; MIPI input; 3A: AE, AF and AWB output; FPN (Fixed Pattern Noise Cancellation); BLC; DPCC; LSC; Bayer-2DNR; Bayer-3DNR; HDR; DRC; DeBayer; CCM/CSM; Gamma; Dehaze/Enhance; 3DLUT; LDCH; 2DNR; Sharp; CGC; output ratio*2; max resolution 4096x2304
Audio unit	I2S S/PDIF	● I2S(8ch) x2, one way for HDMI, support 8 channel transmit and 8 channel receive, I2S(2ch) x2, support 2 channel transmit and 2 channel receive, maximum sample rate 192KHz, support master or slave mode, support 3 I2S formats, support 4 PCM formats, I2S and PCM can not be used at the same time, audio resolution from 16 bit to 32 bit. ● SPDIF x1 support two 16bit audio data stored in a 32bit wide location, support dual phase format stereo audio data output, support linear PCM mode for 16, 20 and 24 bit audio data transfer
	PDM/TDM	● PDM: up to 8 channels, audio resolution from 16-bit to 24-bit, maximum sample rate 192KHz, support master-slave mode; ● TDM: up to 8 channels transmit and 8 channels receive, audio resolution from 16-bit to 24-bit, maximum sample rate 192KHz, support master-slave mode, support 3 I2S formats, support 4 PCM formats.
	DAC(Digital audio codecs)	● Support 3-channel digital ADC and 2-channel digital DAC; support I2S/PCM interface and master-slave mode; support 4-channel audio transmit and 2-channel audio receive respectively in I2S mode; support 2-channel audio transmit or receive in PCM mode; support 16~24-bit sampling rate and three sets of sampling rate between digital ADC and DAC（Group 0：8KHz/16KHz/32KHz/64KHz/128KHz；Group 1：11.025KHz /22.05KHz

		/44.1KHz/ 88.2KHz/ 176.4KHz；Group 2：12KHz/24KHz/48KHz/96KHz/192KHz）
	VAD（Sound status detection）	● Supports I2S/PDM voice data reading; supports voice amplitude detection; supports multi-microphone array data storage; supports one standard interrupt.
Interface	PCIE	● PCIE3.0*1: supports PCIE3.1 protocol and is backward compatible with PCIE2.1 and PCIE1.1 protocols; supports two lane.Support X1 and X2 mode: Compatible with PCIE base specification V3.0, support 2.5Gbps, 5Gbps and 8Gbps per lane per direction serial data rate, X1 (1lane) support RC operation mode, X2 (2lane) support RC and EP operation mode
	USB	● USB3.0*2(Contain OTG)，USB2.0*2(HS-480Mbps,FS-12Mbps,LS-1.5Mbps)
	ENET	● RGMII&RMII*2，Full/half duplex support, VLAN tag detection for IEEE802.1Q receive frames, LAN wakeup architecture and AMD packet architecture, IPv4 headers and TCP/UDP/ICMP checksums, TSO and UFO offload
	Multi PHY	● PCIE2.1*1: 2.5Gbps, 5Gbps support ● SATA3.0*3: 1.5Gb/s, 3.0Gb/s, 6Gb/s, compatible with ATA 3.3 and AHCI revision 1.3.1 ● QSGMII/SGMII:SGMII mode with 1000Mbps ● Support USB3.0 xHCI host controller and DRD controller
	CAN/CANFD	● CAN *3
	UART	● UART*10, both containing two 64-byte FIFOs for transmit and receive operations, programmable baud rate and non-integer clock divider, supports 5 to 8-bit width transmission, supports interrupt-based or DMA-based modes ● Support 115.2Kbps、460.8Kbps、921.6Kbps、1.5Mbps、3Mbps、4Mbps ● UART0/UART1/UART3/UART4/UART5 Support automatic flow control mode ● UART2 DEBUG
	I2C	● I2C*6，7- and 10-bit address modes, programmable clock frequency ● Standard mode: 100Kbit/S，Quick mode: 400Kbit/S
	SPI	● SPI*4

2.2. Hardware Resources

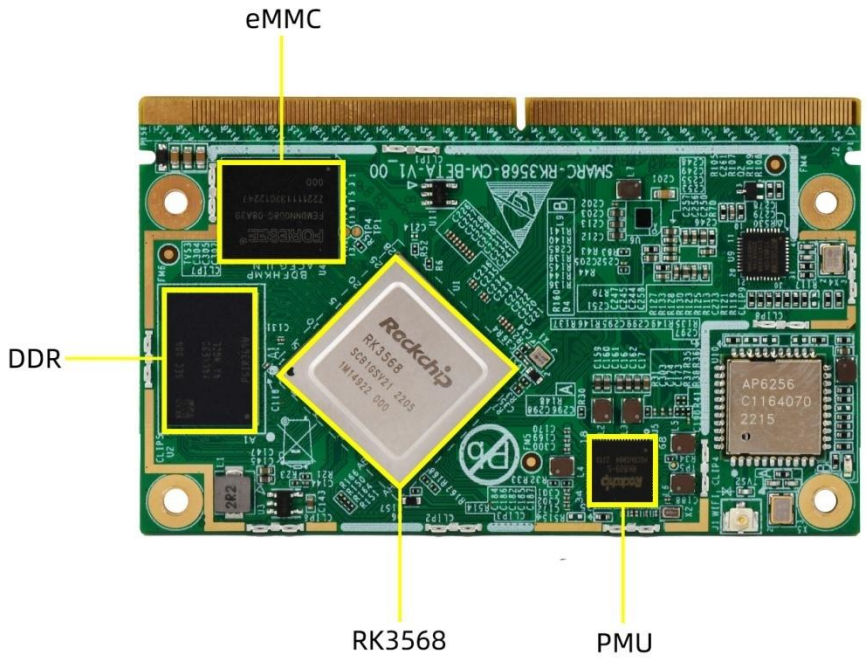
SOM Resources	CPU	RockChip RK3568
	Processor	Quad ARM® Cortex™-A55 cores，RK3568 main frequency up to 2.0GHz
	GPU	Mali-G52-2EE Support OpenGL ES 1.1/2.0/3.2，OpenCL 2.0，Vulkan 1.1 Embedded with high performance 2D acceleration hardware
	VPU	Support 4K 60fps H.265/H.264/VP9 video decoding Support 1080P 60fps H.265/H.264 video encoding Support 8M ISP, support HDR
	NPU	Neural processor unit: supports 1TOPS
	RAM	2GB LPDDR4,(4GB LPDDR4 Optional)
	Flash	8GB eMMC (16GB eMMC,32GB eMMC optional)
	PMIC	RockChip RK809 Power Management Unit
	Ethernet	2-CH network chip with RGMII mode perfectly supports 10M/100M/1000M Ethernet
	WiFi	On-board WiFi module, supports 2.4GHz/5GHz dual-band WiFi, 802.11a/b/g/n/ac protocol
Carrier Board Resrouces	Communication Interface	1 UART debug port (RS232)
		4-CH RS232 serial port (3-wire RS232 serial port)
		1-CH RS485
		2-CH CAN (Extended Frame CAN'T use)
	Display	1-CH Dual Channel LVDS display port ,the resolution is up to 1080P@60Hz
		1-CH HDMI display port (HDMI2.0), the resolution is up to 4096x2304@60Hz
		1-CH eDP display port ,the resolution is up to 2560x1600@60Hz
	Audio	Dual channel stereo -Speaker
		Single channel stereo -Headphone
		Single channel -Mic
	USB	3-CH USB2.0 HOST port
		1-CH USB Type-c port

	Camera	2-CH MIPI-CSI (4-channel), it supports 2-ch camera input ,the resolution supports 2*1080p@80Hz.
	Input	Standard I2C capacitive touch panel
	Extension Port	M.2 B-KEY port (USB3.0) to connect 4G/5G module
		M.2 M-KEY port (PCIE3.0) to connect SSD module
	Storage	1-CH TF card socket
		1-CH SATA
	Others	Reset, Watchdog, Real Time Clock
	Power Input	+12V DC
SDK	Development Tools	Development environment: VM15.5.0 + Ubuntu20.04 or other Linux environment
		Debugging tools for application development use
		Cross-compiler
		Common terminal development and debugging tools
	System images	Image file of the corresponding operating system
	Test programs	Interface application demo test program and test program source code
	Source Code	Bootloader, kernel, file system source code
	Manuals	Hardware manuals, test manuals, device manuals, etc.
	Schematics	Schematic diagram of the Carrier Board (PDF file)
	Mechanical diagram	Carrier Board structure dimensional drawing (DXF file)
Electrical Characteristics	Board layer/size	SOM Size:50mm*82mm,10-layer high precision immersion gold process
		Carrier Board Size:140mm*200mm,4-layer high precision immersion gold process
	Power Consumption	Whole Board Power Consumption <3W (Non-loaded)
	Operating Temperature	0℃ ~ +60℃ (-40℃ ~ +85℃ Optional)
	Storage Temperature	0℃ ~ +70℃
	Operating Humidity	10%~90%, non-condensing

	SOM Configuration	Standard Configuration:2GB DDR/8GB eMMC
		Optional Configuration:4GB DDR/16GB eMMC

2.3. SOM Resources

SMARC-RK3568-CM SOM adopts 10-layer PCB with high-precision immersion gold process and high TG board, which has reliable electrical performance and anti-interference performance; integrated with CPU, LPDDR4, eMMC, power management chip, etc.; By using the SMARC connector to lead out the hardware resources of RK3568 processor, and fully expand the resources of RK3568 processor; The user could make the tailored carrier board by combining different multiplexed pins.



Pic 2

◆Onboard with Rockchip RK3568 processor;

◆Onboard with 2GB LPDDR4, 8GB eMMC (default configuration).

◆SOM adopts 10-layer PCB high precision immersion gold process;

◆SOM Size: 50mm*82mm, suits for different embedded applications;

◆SOM adopts SMARC standard pins to lead out the SOM resources, which complies with SMARC 2.1.

◆By using 5V DC, it has power management chipset on board.

◆Onboard with WIFI module, it supports IEEE802.11 a/b/g/n/ac;

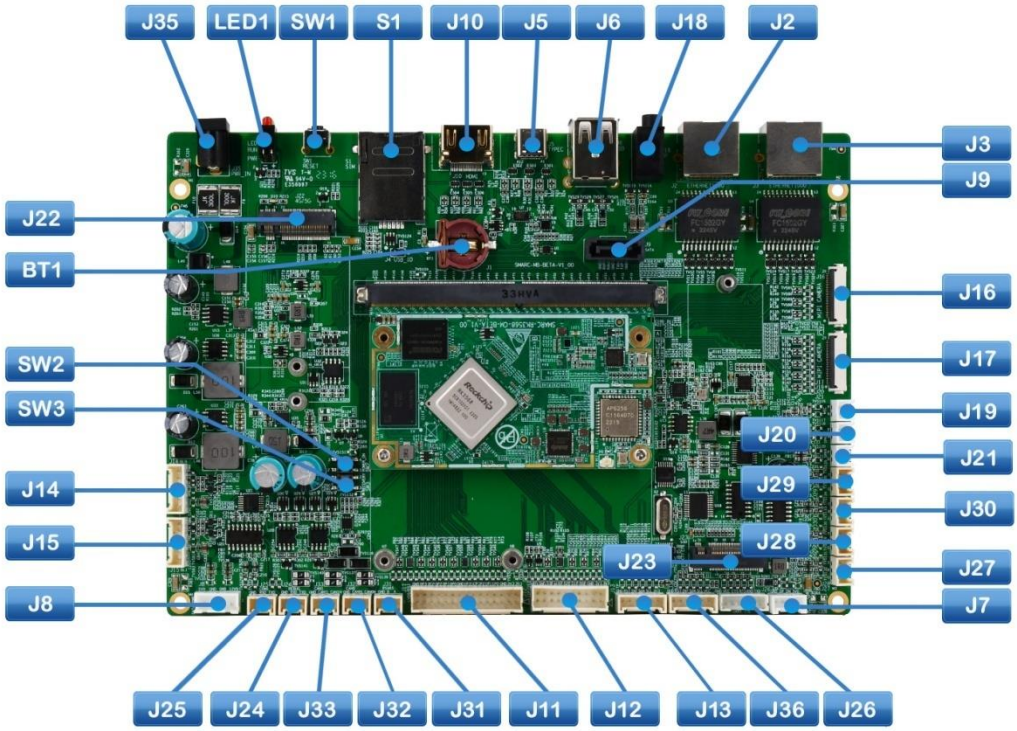
◆Onboard with 2-ch Ethernet chipset;

◆OS:Debian10.0; Android 11.0 ;

The signals from SOM to Carrier Board:

III.Carrier Board Interfaces

Top Side



Pic 3

3.1 Basic Functions

Label #	Function
J35	DC 12V Power In
LED1	Power Indicator, System Operation Indicator
SW1	RESET
S1	SIM Card Socket
J10	HDMI Output
J5	Type-c
J6	USB2.0 HOST (2*USB2.0)
J18	3.5mm HP connector
J2	Gigabit Ethernet Port
J3	Gigabit Ethernet Port
J9	SATA 3.0
J16	MIPI_CSI
J17	MIPI_CSI
J19	MIC
J20	Speaker_ Left
J21	Speaker_ Right
J29	RS-232
J30	RS-232
J28	RS-232
J27	RS-232
J23	M.2_M-KEY(PCIE3.0 protocol)
J7	USB2.0
J26	Full functional TTL
J36	I2C port (TP)
J13	I2C port (TP)
J12	EDP
J11	Dual channel LVDS port

J31	RS-485
J32	CAN
J33	CAN
J24	Debug port (RS-232)
J25	RK3568_RS232\I.MX8MP_M7_Debug port (RS232)
J8	SATA 3.0
J15	Backlight port
J14	Backlight port
SW3	Recovery
SW2	Power Button
BT1	RTC Button Cell
J22	M.2_B-KEY (USB3.0 protocol)

3.2. PIN Definition

SMARC PIN Definition:

PIN#	Signal Name	Function	IO	Level
P1	NC			
P2	GND			
P3	MIPI_CSI_RX_CLK1P	CSI differential signal		Protocol level
P4	MIPI_CSI_RX_CLK1N			
P5	NC			
P6	NC			
P7	MIPI_CSI_RX_D2P	CSI differential signal		Protocol level
P8	MIPI_CSI_RX_D2N			
P9	GND			
P10	MIPI_CSI_RX_D3P	CSI differential signal		Protocol level
P11	MIPI_CSI_RX_D3N			
P12	GND			
P13	NC			
P14	NC			
P15	GND			
P16	NC			
P17	NC			
P18	GND			
P19	ENET0_TRX3_N	MDI		Protocol level
P20	ENET0_TRX3_P			
P21	ENET0_LED1	LAN Indicator		3.3V
P22	ENET0_LED2			

P23	ENET0_TRX2_N	MDI		Protocol level
P24	ENET0_TRX2_P			
P25	ENET0_LED0	LAN Indicator		3.3V
P26	ENET0_TRX1_N	MDI		Protocol level
P27	ENET0_TRX1_P			
P28	NC			
P29	ENET0_TRX0_N	MDI		Protocol level
P30	ENET0_TRX0_P			
P31	NC			
P32	GND			
P33	SDMMC0_WP	SDIO Write-protection	GPIO0_A0	3.3V, pulled up
P34	SDMMC0_CMD	SDIO Command	GPIO2_A1	1.8V/3.3, default :3.3V
P35	SDMMC0_DET_L	SDIO Determine	GPIO0_A4	3.3V, pulled up
P36	SDMMC0_CLK	SDIO Clock	GPIO2_A2	1.8V/3.3, default 3.3V
P37	SDMMC0_PWREN	SDIO Power Enable	GPIO0_A5	3.3V
P38	GND			
P39	SDMMC0_D0	SDIO Data	GPIO1_D5	1.8V/3.3, default :3.3V
P40	SDMMC0_D1		GPIO1_D6	1.8V/3.3, default :3.3V
P41	SDMMC0_D2		GPIO1_D7	1.8V/3.3, default :3.3V
P42	SDMMC0_D3		GPIO2_A0	1.8V/3.3, default :3.3V
P43	SPI0_CS0_M0	SPI Chip Select	GPIO0_C6	1.8V/3.3, default :3.3V
P44	SPI0_CLK_M0	SPI Clock	GPIO0_B5	1.8V/3.3, default :3.3V
P45	SPI0_MISO_M0	SPI Master Input/ Slaver Output	GPIO0_C5	1.8V/3.3, default :3.3V
P46	SPI0_MOSI_M0	SPI Master Output/ Slaver Input	GPIO0_B6	1.8V/3.3, default :3.3V
P47	GND			

P48	SATA_TXP	SATA Data		Protocol Level
P49	SATA_TXN			
P50	GND			
P51	SATA_RXP	SATA Data		Protocol Level
P52	SATA_RXN			
P53	GND			
P54	FSPI_CS0n	SPI Chip Selection	GPIO1_D3	1.8V
P55	NC			
P56	FSPI_CLK	SPI Clock	GPIO1_D0	1.8V
P57	FSPI_D1	SPI Data	GPIO1_D2	1.8V
P58	FSPI_D0		GPIO1_D1	1.8V
P59	GND			
P60	USB2_HOST3_DP	USB2.0		Protocol Level
P61	USB2_HOST3_DM			
P62	NC			
P63	NC			
P64	NC			
P65	USB2_HOST2_DP	USB2.0		Protocol Level
P66	USB2_HOST2_DM			
P67	NC			
P68	GND			
P69	USB3_HOST1_DP	USB2.0		Protocol Level
P70	USB3_HOST1_DM			
P71	NC			
P72	NC			

P73	PCIE20_WAKEn	PCIE2.0 Wake Up	GPIO1_B1	3.3V
P74	NC			
P75	PCIE30X2_PERSTn_M1	PCIE2.0 复位	GPIO2_D6	3.3V
P76	NC			
P77	PCIE20_CLKREQn_M2	PCIE2.0 Clock Interruption	GPIO1_B0	3.3V
P78	PCIE30X2_CLKREQn_M1	PCIE 3.0 Clock Interruption	GPIO2_D4	3.3V
P79	GND			
P80	PCIE20_REFCLKP	PCIE2.0 Clock Reference		Protocol Level
P81	PCIE20_REFCLKN			
P82	GND			
P83	PCIE30_CLK_P_IN	PCIE3.0 Clock Reference Input		Protocol Level
P84	PCIE30_CLK_N_IN			
P85	GND			
P86	PCIE30_RX0_P	PCIE3.0 Data		Protocol Level
P87	PCIE30_RX0_N			
P88	GND			
P89	PCIE30_TX0_P	PCIE3.0 Data		Protocol Level
P90	PCIE30_TX0_N			
P91	GND			
P92	HDMI_TX2P	HDMI Data		Protocol Level
P93	HDMI_TX2N			
P94	GND			
P95	HDMI_TX1P	HDMI Data		Protocol Level
P96	HDMI_TX1N			
P97	GND			

P98	HDMI_TX0P	HDMI Data		Protocol Level
P99	HDMI_TX0N			
P100	GND			
P101	HDMI_TXCP	HDMI Data		Protocol Level
P102	HDMI_TXCN			
P103	GND			
P104	HDMI_TX_HPDIN	HDMI Hot Swap		1.8V
P105	HDMITX_SCL	HDMI I2C Bus	GPIO4_C7	1.8V, pulled up
P106	HDMITX_SDA		GPIO4_D0	1.8V, pulled up
P107	HDMITX_CEC_M0	HDMI Control	GPIO4_D1	1.8V
P108	GPIO_CAM0_nPWR	Camera power, reset function GPIO	GPIO2_D0	1.8V/3.3, default :1.8V
P109	GPIO_CAM1_nPWR		GPIO2_D1	1.8V/3.3, default :1.8V
P110	GPIO_CAM0_nRST		GPIO3_A2	1.8V/3.3, default :1.8V
P111	GPIO_CAM1_nRST		GPIO3_A4	1.8V/3.3, default :1.8V
P112	GPIO04	GPIO	GPIO2_D7	1.8V/3.3, default :1.8V
P113	PWM4_OUT	PWM	GPIO0_C4	1.8V/3.3, default :1.8V
P114	SPI1_MISO_M1	SPI Master Input/ Slaver Output	GPIO3_C2	1.8V/3.3, default :1.8V
P115	SPI1_MOSI_M1	SPI Master Output/ Slaver Input	GPIO3_C1	1.8V/3.3, default :1.8V
P116	SPI1_CLK_M1	SPI Clock	GPIO3_C3	1.8V/3.3, default :1.8V
P117	PCIE30X1_PERSTn_M1	PCIE3.0 Reset	GIPO3_A1	1.8V/3.3, default :1.8V
P118	PCIE30X1_CLKREQn_M1	PCIE3.0 Clock Interruption	GPIO2_D2	1.8V/3.3, default :1.8V
P119	PCIE30X1_WAKEn_M1	PCIE3.0 Wake up	GPIO2_D3	1.8V/3.3, default :1.8V
P120	GND			
P121	NC			
P122	NC			

P123	NC			
P124	NC			
P125	NC			
P126	GPIO_nRST_OUT	Reset Output _GPIO	GPIO3_B0	1.8V/3.3, default :1.8V
P127	SYS_RESETn	System Reset		3.3V, pulled up
P128	PMIC_PWRON	ON/OFF		3.3V, pulled up
P129	UART7_TX_M1	UART	GPIO3_C4	1.8V/3.3, default :1.8V
P130	UART7_RX_M1		GPIO3_C5	
P131	NC			
P132	NC			
P133	GND			
P134	UART3_TX_M1	UART	GPIO3_B7	1.8V/3.3, default :1.8V
P135	UART3_RX_M1		GPIO3_C0	
P136	UART0_TX	UART	GPIO0_C1	1.8V/3.3, default :1.8V
P137	UART0_RX		GPIO0_C0	
P138	UART0_RTSn		GPIO0_C4	1.8V/3.3, default :1.8V
P139	UART0_CTSn		GPIO0_C7	
P140	UART2_TX_M0	UART	GPIO0_D1	1.8V/3.3, default :1.8V
P141	UART2_RX_M0		GPIO0_D0	
P142	GND			
P143	CAN0_TX_M0	CAN	GPIO0_B3	1.8V/3.3, default :1.8V
P144	CAN0_RX_M0		GPIO0_B4	
P145	CAN1_TX_M0	CAN	GPIO1_A1	1.8V/3.3, default :1.8V
P146	CAN1_RX_M0		GPIO1_A0	
P147	5V0	SOM 5V DC Power In		

P148	5V0			
P149	5V0			
P150	5V0			
P151	5V0			
P152	5V0			
P153	5V0			
P154	5V0			
P155	5V0			
P156	5V0			
S1	I2C4_SCL_M0	I2C	GPIO4_B3	1.8V, pulled up
S2	I2C4_SDA_M0		GPIO4_B2	
S3	GND			
S4	NC			
S5	I2C2_SCL_M1	I2C	GPIO4_B5	1.8V, pulled up
S6	CIF_CLKOUT	Clock Output	GPIO4_C0	1.8V
S7	I2C2_SDA_M1	I2C	GPIO4_B4	1.8V, pulled up
S8	MIPI_CSI_RX_CLK0P	CSI Differential signal		Protocol level
S9	MIPI_CSI_RX_CLK0N			
S10	GND			
S11	MIPI_CSI_RX_D0P	CSI Differential signal		Protocol level
S12	MIPI_CSI_RX_D0N			
S13	GND			
S14	MIPI_CSI_RX_D1P	CSI Differential signal		Protocol level
S15	MIPI_CSI_RX_D1N			
S16	GND			

S17	ENET1_TRX0_P	MDI		Protocol level
S18	ENET1_TRX0_N			
S19	ENET1_LED1	LAN Indicator		3.3V, pulled up
S20	ENET1_TRX1_P	MDI		Protocol level
S21	ENET1_TRX1_N			
S22	ENET1_LED2	LAN Indicator		3.3V, pulled up
S23	ENET1_TRX2_P	MDI		Protocol level
S24	ENET1_TRX2_N			
S25	GND			
S26	ENET1_TRX3_P	MDI		Protocol level
S27	ENET1_TRX3_N			
S28	NC			
S29	NC			
S30	NC			
S31	ENET1_LED0	LAN Indicator		3.3V, pulled up
S32	NC			
S33	NC			
S34	GND			
S35	NC			
S36	NC			
S37	USB3_OTG0_VBUSDET	USB3.0 Device Input Detection		5V
S38	I2S1_MCLK_M0	I2S	GPIO1_A2	1.8V/3.3, default :1.8V
S39	I2S1_LRCK_TX_M0		GPIO1_A5	
S40	I2S1_SDO0_M0		GPIO1_A7	
S41	I2S1_SDI0_M0		GPIO1_B3	

S42	I2S1_SCLK_TX_M0		GPIO1_A3	
S43	NC			
S44	NC			
S45	NC			
S46	NC			
S47	GND			
S48	I2C3_SCL_M1	I2C Bus	GPIO3_B5	1.8V/3.3, default :1.8V, pulled up
S49	I2C3_SDA_M1		GPIO3_B6	
S50	NC			
S51	NC			
S52	NC			
S53	NC			
S54	NC			
S55	NC			
S56	FSPI_D2	SPI Data	GPIO1_C7	1.8V
S57	FSPI_D3		GPIO1_D4	1.8V
S58	NC			
S59	NC			
S60	NC			
S61	GND			
S62	USB3_OTG0_SSTXP	USB3.0		Protocol level
S63	USB3_OTG0_SSTXN			
S64	GND			
S65	USB3_OTG0_SSRXP	USB3.0		Protocol level
S66	USB3_OTG0_SSRXN			

S67	GND			
S68	USB3_OTG0_DP	USB3.0		Protocol level
S69	USB3_OTG0_DM			
S70	GND			
S71	USB3_HOST1_SSTXP	USB3.0		Protocol level
S72	USB3_HOST1_SSTXN			
S73	GND			
S74	USB3_HOST1_SSRXP	USB3.0		Protocol level
S75	USB3_HOST1_SSRXN			
S76	PCIE20_PERSTn	PCIE2.0 Reset	GPIO1_B2	1.8V/3.3, default :3.3V
S77	NC			
S78	PCIE20_RXP	PCIE2.0 Data		Protocol level
S79	PCIE20_RXN			
S80	GND			
S81	PCIE20_TXP	PCIE2.0 Data		Protocol level
S82	PCIE20_TXN			
S83	GND			
S84	NC			
S85	NC			
S86	GND			
S87	PCIE30_RX1P	PCIE3.0 Data		Protocol level
S88	PCIE30_RX1N			
S89	GND			
S90	PCIE30_TX1P	PCIE3.0 Data		Protocol level
S91	PCIE30_TX1N			

S92	GND			
S93	EDP_TX_D0P	EDP		Protocol level
S94	EDP_TX_D0N			
S95	NC			
S96	EDP_TX_D1P	EDP		Protocol level
S97	EDP_TX_D1N			
S98	EDP_HPDIN_M1		GPIO0_C2	1.8V/3.3, default :1.8V
S99	EDP_TX_D2P			Protocol level
S100	EDP_TX_D2N			
S101	GND			
S102	EDP_TX_D3P	EDP		Protocol level
S103	EDP_TX_D3N			
S104	USB3_OTG0_ID	USB3.0 OTG ID		3.3V
S105	EDP_TX_AUXP	EDP		Protocol level
S106	EDP_TX_AUXN			
S107	GPIO_LCD1_BKLT_EN	LCD backlight enables GPIO	GPIO3_A7	1.8V/3.3, default :1.8V
S108	MIPI_DSI_TX1_CLKP	DSI differential signal		Protocol level
S109	MIPI_DSI_TX1_CLKN			
S110	GND			
S111	MIPI_DSI_TX1_D0P	DSI differential signal		Protocol level
S112	MIPI_DSI_TX1_D0N			
S113	NC			
S114	MIPI_DSI_TX1_D1P	DSI differential signal		Protocol level
S115	MIPI_DSI_TX1_D1N			
S116	GPIO_LCD1_VDD_EN	LCD power enables GPIO	GPIO3_A3	1.8V/3.3, default :1.8V

S117	MIPI_DSI_TX1_D2P	DSI differential signal		Protocol level
S118	MIPI_DSI_TX1_D2N			
S119	GND			
S120	MIPI_DSI_TX1_D3P	DSI differential signal		Protocol level
S121	MIPI_DSI_TX1_D3N			
S122	LCD1_BKLT_PWM	LCD Backlight PWM	GPIO3_B2	1.8V/3.3, default :1.8V
S123	GPIO13	GPIO	GPIO3_A6	1.8V/3.3, default :1.8V
S124	GND			
S125	MIPI_DSI_TX0_D0P/LVDS_TX0_D0 P	DSI multiplexed with LVDS		Protocol level
S126	MIPI_DSI_TX0_D0N/LVDS_TX0_D 0N			
S127	GPIO_LCD0_BKLT_EN		GPIO3_A5	1.8V/3.3, default :1.8V
S128	MIPI_DSI_TX0_D1P/LVDS_TX0_D1 P			Protocol level
S129	MIPI_DSI_TX0_D1N/LVDS_TX0_D 1N			
S130	GND			
S131	MIPI_DSI_TX0_D2P/LVDS_TX0_D2 P	DSI multiplexed with LVDS		Protocol level
S132	MIPI_DSI_TX0_D2N/LVDS_TX0_D 2N S133 LCD0_VDD_E			
S133	GPIO_LCD0_VDD_EN	LCD power enables GPIO	GPIO1_A6	1.8V/3.3, default :1.8V
S134	MIPI_DSI_TX0_CLKP/LVDS_TX0_ CLKP	DSI multiplexed with LVDS		Protocol level
S135	MIPI_DSI_TX0_CLKN/LVDS_TX0_ CLKN			
S136	GND			
S137	MIPI_DSI_TX0_D3P/LVDS_TX0_D3 P	DSI multiplexed with LVDS		Protocol level
S138	MIPI_DSI_TX0_D3N/LVDS_TX0_D 3N			

S139	I2C5_SCL_M0	I2C	GPIO3_B3	1.8V/3.3, default :1.8V,
S140	I2C5_SDA_M0		GPIO3_B4	pulled up
S141	LCD0_BKLT_PWM	LCD Backlight PWM	GPIO3_B1	1.8V/3.3, default :1.8V
S142	GPIO12	GPIO	GPIO1_A4	1.8V/3.3, default :1.8V
S143	GND			
S144	NC			
S145	NC			
S146	PCIE30X2_WAKEn_M1	PCIE3.0 wake up	GPIO2_D5	3.3V
S147	VCC_RTC_3V0			
S148	NC			
S149	GPIO_SLEEP	GPIO Sleep	GPIO0_B7	1.8V/3.3, default :1.8V
S150	GPIO_PWR_BAD	GPIO Power failure	GPIO0_D5	1.8V
S151	NC			
S152	NC			
S153	GPIO_CARR_nSTBY	GPIO Output	GPIO0_D3	1.8V
S154	GPIO_CARR_PWRON	GPIO Output	GPIO0_D4	1.8V
S155	RECOVERY	Burn-in button		1.8V
S156	NC			
S157	NC			
S158	GND			

J16: MIPI_CSI

PIN#	Signal Name
1	VCC_CAM0_5V0
2	GND

3	VCC_CAM0_3V3
4	VCC_CAM0_3V3
5	GND
6	CSI0_CK_N
7	CSI0_CK_P
8	GND
9	CSI0_RX0_N
10	CSI0_RX0_P
11	GND
12	CSI0_RX1_N
13	CSI0_RX1_P
14	GND
15	NC
16	NC
17	GND
18	NC
19	NC
20	GND
21	CSI0_I2C_SDA
22	CSI0_I2C_SCL
23	CSI0_PWDN
24	CSI0_nRST
25	GND
26	CSI0_PWR_EN

J17: MIPI_CSI

PIN#	Signal Name
1	VCC_CAM1_5V0
2	GND
3	VCC_CAM1_3V3
4	VCC_CAM1_3V3
5	GND
6	CSI1_CK_N
7	CSI1_CK_P
8	GND
9	CSI1_RX0_N
10	CSI1_RX0_P
11	GND
12	CSI1_RX1_N
13	CSI1_RX1_P
14	GND
15	NC
16	NC
17	GND
18	NC
19	NC
20	GND
21	CSI1_I2C_SDA
22	CSI1_I2C_SCL
23	CSI1_PWDN
24	CSI1_nRST

25	GND
26	CSI1_PWR_EN

J19: MIC

PIN#	Signal Name
1	AUD_MIC+
2	AUD_MIC-

J20: Speaker_ Left

PIN#	Signal Name
1	AUD_AMP_OUTPL
2	AUD_AMP_OUTNL

J21: Speaker_ Right

PIN#	Signal Name
1	AUD_AMP_OUTPR
2	AUD_AMP_OUTNR

J29/J30/J28/J27: RS-232

PIN#	Signal Name
1	COM_TX
2	COM_RX
3	GND

J7: USB2.0

PIN#	Signal Name
1	VCC_EXT_5V0
2	USB5_DN_CON
3	USB5_DP_CON

4	GND

J26： TTL Port

PIN#	Signal Name
1	TXD_TTL
2	RXD_TTL
3	RTS_TTL
4	CTS_TTL
5	VCC_IO
6	GND

J23: M.2_M-KEY(PCIE3.0 Protocol）

Signal Name	PIN#	PIN#	Signal Name
GND	1	2	VCC_SSD_3V3
GND	3	4	VCC_SSD_3V3
NC	5	6	NC
NC	7	8	NC
GND	9	10	LED
NC	11	12	VCC_SSD_3V3
NC	13	14	VCC_SSD_3V3
GND	15	16	VCC_SSD_3V3
NC	17	18	VCC_SSD_3V3
NC	19	20	NC
GND	21	22	NC
NC	23	24	NC
NC	25	26	NC

GND	27	28	NC
NC	29	30	NC
NC	31	32	NC
GND	33	34	NC
NC	35	36	NC
NC	37	38	NC
GND	39	40	VCC_SSD_3V3
SSD_PET0_N	41	42	VCC_SSD_3V3
SSD_PET0_P	43	44	NC
GND	45	46	NC
SSD_PER0_N	47	48	NC
SSD_PER0_P	49	50	PCIE_A_nRST
GND	51	52	PCIE_A_nCKREQ
SSD_REFCLK_N	53	54	PCIE_nWAKE
SSD_REFCLK_P	55	56	NC
GND	57	58	NC
STD M-KEY	• • •	• • •	STD M-KEY
NC	67	68	NC
NC	69	70	VCC_SSD_3V3
GND	71	72	VCC_SSD_3V3
GND	73	74	VCC_SSD_3V3
GND	75		

J36: I2C（TP）

PIN#	Signal Name
1	VCC_IO

2	I2C2_SCL
3	I2C2_SDA
4	GPIO_LCD0_nINT
5	GPIO_LCD0_nRST
6	GND

J13: I2C（TP）

PIN#	Signal Name
1	VCC_EXT_3V3
2	TP_I2C_SCL
3	TP_I2C_SDA
4	TP_nINT
5	TP_nRST
6	GND

J12: EDP

Signal Name	PIN#	PIN#	Signal Name
VCC_LCD_5V0	1	2	VCC_LCD_3V3
VCC_LCD_5V0	3	4	VCC_LCD_3V3
GND	5	6	GND
LCD2_D0_N	7	8	LCD2_D0_P
LCD2_D1_N	9	10	LCD2_D1_P
LCD2_D2_N	11	12	LCD2_D2_P
LCD2_AUX_N	13	14	LCD2_AUX_P
LCD2_D3_N	15	16	LCD2_D3_P
GND	17	18	GND
LCD2_nRST	19	20	LCD2_HPD

J11： Dual Channel LVDS

Signal Name	PIN#	PIN#	Signal Name
VCC_LCD_5V0	1	2	VCC_LCD_3V3
VCC_LCD_5V0	3	4	VCC_LCD_3V3
GND	5	6	GND
LCD1_D0_N	7	8	LCD1_D0_P
LCD1_D1_N	9	10	LCD1_D1_P
LCD1_D2_N	11	12	LCD1_D2_P
LCD1_CK_N	13	14	LCD1_CK_P
LCD1_D3_N	15	16	LCD1_D3_P
GND	17	18	GND
LCD0_D0_N	19	20	LCD0_D0_P
LCD0_D1_N	21	22	LCD0_D1_P
LCD0_D2_N	23	24	LCD0_D2_P
LCD0_CK_N	25	26	LCD0_CK_P
LCD0_D3_N	27	28	LCD0_D3_P
GND	29	30	GND

J31：RS-485

PIN#	Signal Name
1	RS485_A
2	RS485_B
3	GND

J32/J33：CAN

PIN#	Signal Name
1	CAN_H

2	CAN_L
3	GND

J24：Debug Port（RS-232）

PIN#	Signal Name
1	COM_TXD
2	COM_RXD
3	GND

J25: Rk3568_RS232\i.MX8MP_M7_Debug (RS232)

PIN#	Signal Name
1	COM_TXD
2	COM_RXD
3	GND

J8: SATA3.0 Power

PIN#	Signal Name
1	VCC_SATA_12V0
2	GND
3	GND
4	VCC_SATA_5V0

J15/J14: Backlight

PIN#	Signal Name
1	VCC_BL
2	VCC_BL
3	GND
4	GND

5	BL0_EN
6	BL0_PWM

J22：M.2_B-KEY（USB3.0）

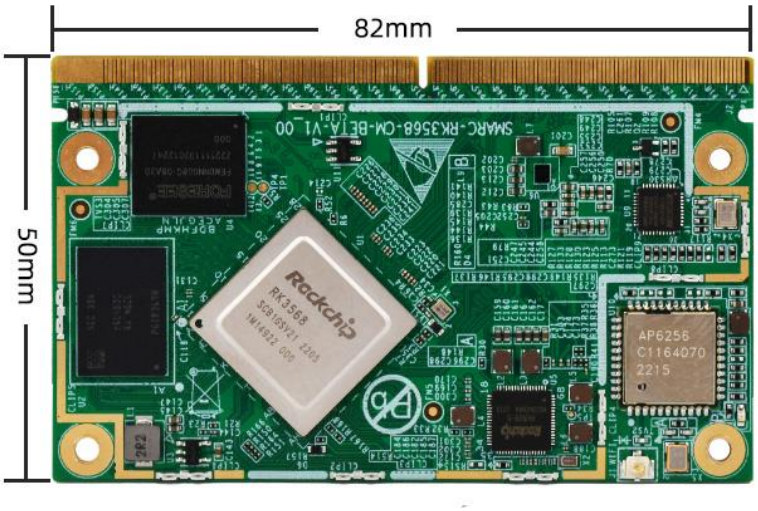
Signal Name	PIN#	PIN#	Signal Name
GND	1	2	VCC_5G_3V8
GND	3	4	VCC_5G_3V8
GND	5	6	5G_ON_OFF
5G_USB_D_P	7	8	5G_DISEN
5G_USB_D_N	9	10	5G_STATE
GND	11	…	STD B-KEY
STD B-KEY	…	20	NC
GND	21	22	NC
NC	23	24	NC
NC	25	26	NC
GND	27	28	NC
5G_USB_SSRX_N	29	30	USIM_nRST
5G_USB_SSRX_P	31	32	USIM_CLK
GND	33	34	USIM_DATA
5G_USB_SSTX_N	35	36	USIM_VDD
5G_USB_SSTX_P	37	38	VCC_EXT_1V8
GND	39	40	NC
NC	41	42	NC
NC	43	44	NC
GND	45	46	NC
NC	47	48	NC

NC	49	50	VCC_EXT_3V3
GND	51	52	VCC_EXT_3V3
NC	53	54	VCC_EXT_3V3
NC	55	56	NC
GND	57	58	NC
NC	59	60	NC
NC	61	62	NC
NC	63	64	NC
NC	65	66	NC
5G_nRST	67	68	NC
GND	69	70	VCC_5G_3V8
GND	71	72	VCC_5G_3V8
GND	73	74	VCC_5G_3V8
NC	75		

IV. Size & Structure

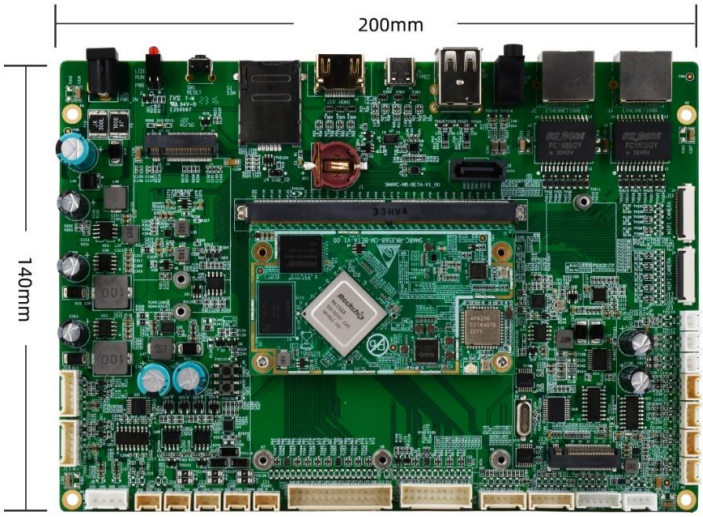
Unit: mm, if need the datasheet for receptacle, please email us: supports@qiyangtech.com

4.1.SOM Size



Pic 5

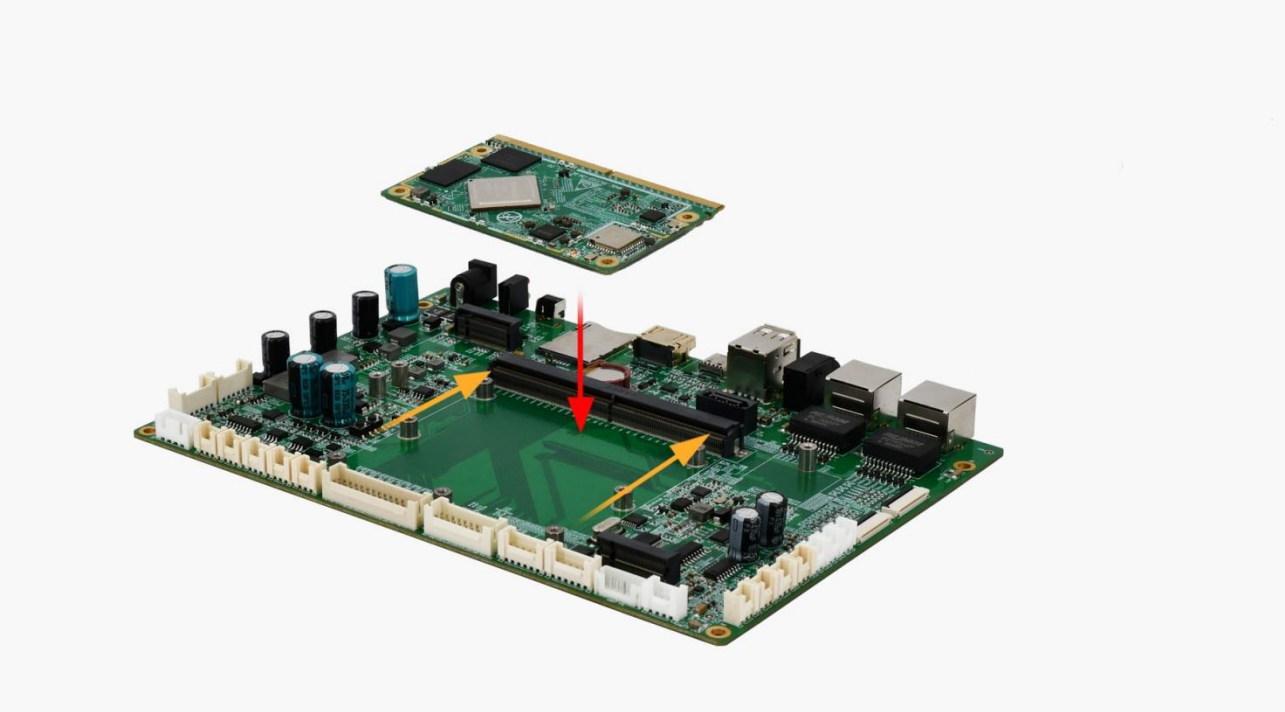
4.2. Carrier Board Size



Pic 6

V. Connection Illustration

Pay attention to the location of the SOM module: (Refer to the below picture)



Pic 7

VI.Electrical Characteristics

Item	Parameters
Working Temperature	0℃ ~+70℃ (-40℃ ~ +85℃ Optional)
Storage Temperature	-10℃ ~+70℃
Humidity	10%~90%, non-condensing
SOM Size	50mm*82mm，10-layer high precision immersion gold process
Carrier Board Size	140mm*200mm, 4-layer high precision immersion gold process
Whole Board Power Consumption	＜3W（No-loaded）
Power Supply	DC12V/2.5A

VII.Software Description

The software support provided by the SMARC-RK3568-KIT mainly includes Linux /Android.

The SMARC-RK3568-KIT Debian Linux User Manual describes in detail the establishment and use of the Linux development environment provided by the SMARC-RK3568-KIT development board, please refer to the related documentation for more details.

The SMARC-RK3568-KIT Android User Manual describes in detail the establishment and use of the Android development environment provided by the SMARC-RK3568-KIT. development board, for more details, please refer to the related documentations.

Ⅷ. Note

1.

- Exceeding the warranty service period.
- No valid purchase documents.
- Into the liquid, moisture or mold.
- Failure and damage caused by non-quality reasons such as dropping, strong vibration or unauthorized alteration or misuse after purchase.
- Damage caused by force majeure.

2. Our company retains the intellectual property rights of all SMARC-RK3568-KIT products with independently developed related software and hardware technical data; users can only use them for teaching, experimental and scientific research purposes, and cannot engage in any commercial use, nor can they distribute them on the network, or tamper with their copyrights by interception or modification.

3. This product accepts customers' bulk order, and the company will provide full technical support and service.

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