IAC-RK3568-KIT

Hardware Manual

Version：V 2.0
2022.8

Technical Support

If you have questions about the documents, you can contact us during office hours (Monday to Friday 8:30-12:00, 13:30-17:30)

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Technical Email：supports@qiyangtech.com

Technical Support Phone：0571-87858811-805

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Information updates

1. Information updates

Product-related manuals and datasheets are constantly being improved and updated; please ensure that they are up-to-date when you use them.

2.Update notice

Qiyang's newest product information and news updates will be released through the WeChat official account, please pay attention!

3.How to get information

After purchase, please contact the relevant sales staff to obtain the SDK.

Version Record

Version	Hardware Platform	Description	Date	Reviser
1.0	IAC-RK3568-MB V1.00	First version	2021-08	wwx
2.0	IAC-RK3568-MB V1.02	1.Change Pictures 2.Update the UART's pin definition	2022-08	wwx

Catalogue

''Notice'': This manual mainly introduces the hardware interface of IAC-RK3568-KIT development board

I. Preface

1.1 Company Profile

Zhejiang Qiyang Intelligent Technology Co., Ltd. was founded in Hangzhou in 2007, is a national high-tech enterprise focusing on the development, production and sales of ARM embedded products. 10 years of accumulation and precipitation, successfully built a product development to mass production service chain.

As the core of the company, Qiyang R&D team consists of more than 30 embedded engineers, dedicated to providing users with easy-to-use embedded hardware, software tools and customized product solutions. It has been widely used in industrial control, Internet of Things, new retail, medical, electric power, environmental monitoring, charging pile and other fields.

The production base in Zhuji provides a strong guarantee for Qiyang, covering an area of 5,000 square meters, with 2 SMT production lines, through and strictly follow the ISO9001 quality management system certification to guide production. Relying on the strong production strength, the annual production capacity can reach 1 million sets to ensure the delivery time of users and solve the worries.

Qiyang has a perfect sales and marketing network, professional sales and after-sales team to provide users with a full range of technical support and services. Business has spread to more than 120 countries and regions, successfully helping more than 2000 users to bring their products to market quickly and efficiently.

The combination and extension of R&D, production capacity and market has laid a solid foundation for Qiyang Intelligence to become a professional and global supplier of embedded software and hardware.

We offer:

- **Multi-platform software/hardware products**

NXP, Rockchip, MTK, Renesas, TI, Atmel, Cirrus Logic and other multi-platform ARM development boards/core boards/industrial control boards and peripheral hardware products, as well as supporting tools and software resources to support rapid secondary development of users.

- **Customized Services**

We fully utilize our accumulated technology on ARM platform and Linux, Android, Ubuntu and Debian operating systems to provide customized embedded product services (OEM/ODM).

Thank you for using Qiyang's products, we will do our best to provide you with technical assistance! Wish you good luck in your work!

1.2 IAC-RK3568-KIT suggestions for using development/evaluation boards

1)Before using the development board, please make sure to read this manual first.

2)Please check the packing list in detail before use, and detect whether there are missing files on the data CD.

3) Understand the basic structure and composition of the development board, including the allocation of hardware resources, the definition of each pin of the core board and the base board, and the definition of the expansion pins, etc..

4) If you need to design and develop under Debian Linux system and program burn-in for the development board, it is recommended to read another document ***IAC-RK3568-KIT Debian Linux User's Manual*** in addition to this document.

5) If you need to design and develop under Android system and program burn-in of the development board, it is recommended to read another document ***IAC-RK3568-KIT Android User's Manual*** in addition to this document.

6) IAC-RK3568-KIT embedded development board, accept bulk orders.

II. System Composition

2.1 Chip Overview

The Rockchip RK3568 processor is a high-performance, low-power quad-core application processor chip designed for personal mobile Internet devices and AIoT devices.

The RK3568 quad-core 64-bit Cortex-A55 processor is clocked at up to 2.0GHz and features a 22nm advanced process.

The RK3568 has a variety of powerful embedded hardware engines built in to provide excellent performance for high-end applications, supporting almost full-format H.264 4k@60fps decoding, H.265 4k@60fps decoding, and also H.264/H.265 1080p@60fps encoding, as well as encoding/decoding of high-quality JPEGs.

The RK3568 has a built-in 3D GPU that is fully compatible with OpenGL ES1.1/2.0/3.2, OpenCL 2.0 and Vulkan 1.0. The dedicated 2D hardware engine will maximize display performance and provide a smooth operating experience.

The embedded NPU supports INT8/INT16 hybrid operation. In addition, with its powerful compatibility, network models based on a range of frameworks such as TensorFlow / MXNet / PyTorch / Caffe can be easily converted.

With a high-performance memory interface (DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X), RK3568 is capable of providing the memory bandwidth required for high-performance scenarios.

The functional block diagram of the processor is as follows：

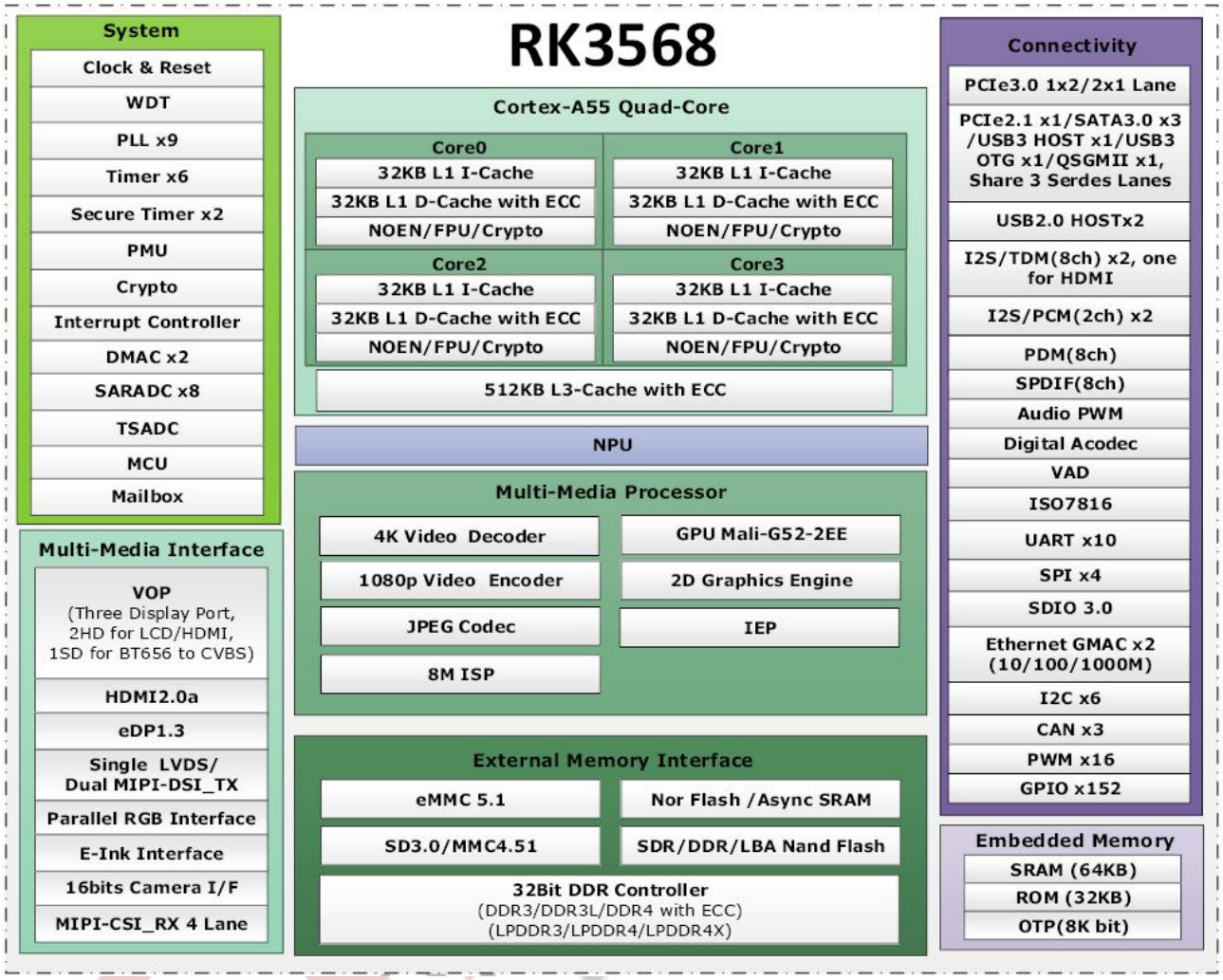

Chart 1

Detailed Parameters Of CPU

CORE	CPU	● Quad-core Arm®Cortex®-A55 2.0GHz ● 32 KB Level 1 instruction cache, 32 KB Level 1 data cache and checksum ● 512 KB same standard Level 3 cache and checksum ● Supports 64bit Armv8 architecture
	MCU	● 32bits microprocessor ● Harvard architecture independent instruction and data memory ● Integrated Programmable Interrupt Controller (IPIC) ● Integrated Debug Controller (DEBUG) and JTAG interface
Storage	On-chip storage	● Boot ROM(32KB)---Bootstrap read-only memory（32KB） ● On-chip SRAM SYSTEM(64KB) + PMU(8KB) --- On-chip static random memory (System 64KB + Power Management Unit 8KB)
	External Storage	● 16/32-bit DRAM interface:LPDDR4/4X,LPDDR3,DDR4,DDR3,DDR3L ● 8-bit Asynchronous/ONFI Synchronous NAND FLASH, Toggle Flash，SLC/MLC/TLC Flash，Hardware ECC ● EMMC 5.1 FLASH(support HS200) Compatible 4.41、4.51、5.0Specification，support 1/4/8bit Data Width ● SD3.0/MMC 4.51，4bit Data Width；SPI FLASH support 1/4/8bit Data Width ● FlexSPI Flash， Serial NOR/Nand Flash，support SDR
On-chip unit	GPU	● Mali-G52 1-Core-2EE ● Support OpenGL ES 1.1, 2.0, and 3.2；Vulkan 1.0 and 1.1；OpenCL 2.0 Full Profile；1600Mpix/s（Megapixels/sec） fill rate when 800MHz clock frequency ● Support 38.4GLOPs（Number of floating point operations） when 800MHz clock frequency
	NPU	● 0.8 TOPS(Trillion times per second)，support INT8/INT16Hybrid operation, Deep Learning Architecture.
	ISP	● Support video data from DVP or MIPI CSI---DVP or MIPI CSI Get video data ● Maximum resolution is 4096x2304---Maximum Resolution 4096x2304
	VPU	Video Decoding (Video Decoder)

		● H.265 HEVC/MVC Main10 Profile yuv420@L5.1 up to 4096x2304@60fps ● VP9 Profile0/2 yuv420@L5.1 up to 4096x2304@60fps ； ● VP8 verision2,up to 1920x1088@60fps； ● VC1 Simple Profile@low, medium, high levels, Main Profile@low, medium, high levels, Advanced Profile@level0~3,up to 1920x1088@60fps ● MPEG-4 Simple Profile@L0~6,Advanced Simple Profile@L0~5,up to 1920x1088@ 60fps ● MPEG-1/2 Main Profile, low, medium and high levels, up to 1920x1088@60fps ● H.264 AVC/MVC Main10 Profile yuv400/yuv420/yuv422/@L5.1 up to 4096x2304@ 60fps ● H.263 Profile0,levels 10-70,up to 720x576@60fps Video Decoding (Video Encoder) ● H.264/AVC BP/MP/HP@level4.2，up to 1920x1080@100fps ● H.265/HEVC MP@level4.1, up to 1920x1080@100fps (4096x4096@10fps with TILE) Support YUV/RGB video source rotation and mirroring
Display Controller	VOP	● Video Input：support 2 cluster layer、2 esmart layer and 2 smart layer,4096X2160 Resolution input，RGB/YUV/YUYV Format，Up and down 4~1/4 scale scaling, rotation, 4 regions ● Overlay （Video Overlay）：Supports up to 6 levels 2 Cluster/2 Esmart/2 Smart,Support RGB/YUV overlay ● POST process（Post-processing）：HDR10/HDR HLG，HDR2SDR/SDR2HDR；3D–LUT/P2 I/CSC/BCSH/DITHER/CABC/GAMMA/COLORBAR ● Write back(Writing Board)：ARGB8888/RGB888/RGB565/YUV420 Format；Maximum Resolution 1920X1080 ● Video Output：Video output 0, up to 4096x2304 @ 60Hz resolution; video output 1, up to 2048x1536 @ 60Hz resolution; video output 2, up to 1920x1080 @ 60Hz resolution
Display Interface	HDMI	● Supports HDMI 1.4 and HDMI 2.0 operation all the way to the physical layer PHY ● Up to 10-bit depth color mode; up to 1080p@120Hz

		and 4096x2304@60Hz resolution; support for 3D video formats; support for HDCP (High-bandwidth Digital Content Protection) 1.4/2.2 protocol ● Supports RGB/YUV (up to 10-bit) format
	LVDS	● Compliant with TIA/EIA-644-A LVDS specification ● LVDS interface supports RGB888 and RGB666 inputs ● Supports VESA/JEIDA LVDS data format transmission
	MIPI DSI	● Compatible with MIPI Alliance Interface Specification V1.2 ● Support dual-channel DSI, each channel supports 4 data lanes ● Each lane supports up to 2.5Gbps rate ● Single MIPI mode: up to 1920x1080@60Hz resolution output; Dual MIPI mode: up to 2560x1440@60Hz resolution output ● Supports RGB (up to 8-bit) format
	eDP	● Supports 1 eDP 1.3 interface, up to 4 physical lanes, 2.7Gbps per lane, up to 2560x1600@60Hz ● Support Panel Self-Refresh (PSR) ● Supports RGB (up to 10-bit) format
	EBC	● Compatible with e-ink screen ● Supports 2200x1650 resolution with 16-bit data lines ● Up to 16 levels of grayscale and 256 frames per scan
	RGB/BT.1120	● Supports up to 1920x1080@60Hz resolution and RGB (up to 8-bit) format; up to 150MHz data rate
	BT.656	● Support PAL and NTSC
Video input interface	MIPI CSI	● Compatible with MIPI Alliance Interface Specification V1.2 ● Up to 4 data lanes, each lane supports up to 2.5Gbps rate ● Support MIPI high-speed mode (MIPI-HS), MIPI low-power mode (MIPI-LP) ● Support two combinations: ① 1 way clock lane and 4 way data lane; ② 2 way data lane with each clock lane
	DVP	● Supports 8-bit/10-bit/12-bit/16-bit input; up to 150MHz data rate input
	VICAP	● Support BT601 YCbCr 422 8-bit input, RAW 8/10/12-bit input, BT656 YCbCr 422 8-bit input, BT1120 YCbCr 422 8/10/12/16-bit input, single/dual edge sampling; 2/4 mixed BT656/BT1120 YCbCr 422 8-bit input; YUYV sequence configuration; support polarized pixel_clk,

		hsync and vsync configuration; support CSI2 data protocol (up to 4 IDs) reception, DSI data protocol (video mode/command mode) reception; window cropping support; virtual step support when writing to DDR; YUV data support NV16/NV12 output; raw data compression/uncompressed output support
	ISP	● DVP input; MIPI input; 3A: AE, AF and AWB output; FPN (Fixed Pattern Noise Cancellation); BLC; DPCC; LSC; Bayer-2DNR; Bayer-3DNR; HDR; DRC; DeBayer; CCM/CSM; Gamma; Dehaze/Enhance; 3DLUT; LDCH; 2DNR; Sharp; CGC; output ratio*2; max resolution 4096x2304
Audio unit	I2S S/PDIF	● I2S(8ch) x2, one way for HDMI, support 8 channel transmit and 8 channel receive, I2S(2ch) x2, support 2 channel transmit and 2 channel receive, maximum sample rate 192KHz, support master or slave mode, support 3 I2S formats, support 4 PCM formats, I2S and PCM can not be used at the same time, audio resolution from 16 bit to 32 bit. ● SPDIF x1 support two 16bit audio data stored in a 32bit wide location, support dual phase format stereo audio data output, support linear PCM mode for 16, 20 and 24 bit audio data transfer
	PDM/TDM	● PDM: up to 8 channels, audio resolution from 16-bit to 24-bit, maximum sample rate 192KHz, support master-slave mode; ● TDM: up to 8 channels transmit and 8 channels receive, audio resolution from 16-bit to 24-bit, maximum sample rate 192KHz, support master-slave mode, support 3 I2S formats, support 4 PCM formats.
	DAC(Digital audio codecs)	● Support 3-channel digital ADC and 2-channel digital DAC; support I2S/PCM interface and master-slave mode; support 4-channel audio transmit and 2-channel audio receive respectively in I2S mode; support 2-channel audio transmit or receive in PCM mode; support 16~24-bit sampling rate and three sets of sampling rate between digital ADC and DAC（Group 0：8KHz/16KHz/32KHz/64KHz/128KHz；Group 1：11.025KHz /22.05KHz /44.1KHz/ 88.2KHz/ 176.4KHz；Group 2：12KHz/24KHz/48KHz/96KHz/192KHz）
	VAD （Sound	● Supports I2S/PDM voice data reading; supports voice

	status detection）	amplitude detection; supports multi-microphone array data storage; supports one standard interrupt.
Interface	PCIE	● PCIE3.0*1: supports PCIE3.1 protocol and is backward compatible with PCIE2.1 and PCIE1.1 protocols; supports two lane.Support X1 and X2 mode: Compatible with PCIE base specification V3.0, support 2.5Gbps, 5Gbps and 8Gbps per lane per direction serial data rate, X1 (1lane) support RC operation mode, X2 (2lane) support RC and EP operation mode
	USB	● USB3.0*2(Contain OTG)，USB2.0*2(HS-480Mbps,FS-12Mbps,LS-1.5Mbps)
	ENET	● RGMII&RMII*2，Full/half duplex support, VLAN tag detection for IEEE802.1Q receive frames, LAN wakeup architecture and AMD packet architecture, IPv4 headers and TCP/UDP/ICMP checksums, TSO and UFO offload
	Multi PHY	● PCIE2.1*1: 2.5Gbps, 5Gbps support ● SATA3.0*3: 1.5Gb/s, 3.0Gb/s, 6Gb/s, compatible with ATA 3.3 and AHCI revision 1.3.1 ● QSGMII/SGMII:SGMII mode with 1000Mbps ● Support USB3.0 xHCI host controller and DRD controller
	CAN/CANFD	● CAN *3
	UART	● UART*10, both containing two 64-byte FIFOs for transmit and receive operations, programmable baud rate and non-integer clock divider, supports 5 to 8-bit width transmission, supports interrupt-based or DMA-based modes ● Support 115.2Kbps、460.8Kbps、921.6Kbps、1.5Mbps、3Mbps、4Mbps ● UART0/UART1/UART3/UART4/UART5 Support automatic flow control mode ● UART2 DEBUG
	I2C	● I2C*6，7- and 10-bit address modes, programmable clock frequency ● Standard mode: 100Kbit/S，Quick mode: 400Kbit/S
	SPI	● SPI*4

2.2 Development Board Resources

Hardware Resources	CPU	RockChip RK3568
	Processor	Quad ARM® Cortex™-A55 cores，RK3568 main frequency up to 2.0GHz
	GPU	Mali-G52 1-Core-2EE Support OpenGL ES 1.1/2.0/3.2，OpenCL 2.0，Vulkan 1.1 Embedded with high performance 2D acceleration hardware
	VPU	Support 4K 60fps H.265/H.264/VP9 video decoding Support 1080P 60fps H.265/H.264 video encoding Support 8M ISP, support HDR
	NPU	Neural processor unit: supports 1TOPS
	RAM	2GB LPDDR4
	Flash	8GB eMMC (16GB eMMC,32GB eMMC optional)
	PMIC	RockChip RK809 Power Management Unit
	Ethernet	2-CH network chip with RGMII mode perfectly supports 10M/100M/1000M Ethernet
	WiFi	On-board WiFi module, supports 2.4GHz/5GHz dual-band WiFi, 802.11a/b/g/n/ac protocol
	Communication Interface	1 UART debug serial port (TTL level)
		2-CH RS232 serial port (3-wire RS232 serial port)
		1-CH RS485 interface
		3-CH CAN interface （Extended Frame CAN'T use）
	Display Interface	2X4-channel MIPI_DSI display interfaces (1 x multiplexed LVDS) with resolutions up to 1920x1080@60Hz
		1 single-channel LVDS display interface, resolution up to 1280x800@60Hz
		1-ch HDMI display interface (HDMI2.0), resolution up to 4096x2160@60Hz
		1-CH eDP display interface, resolution up to 2560x1600@60Hz
	Audio Interface	Audio (amplifier) output interface
		Two-channel audio output (Earphone socket)
		Single-channel MIC audio input
	USB Interface	2-CH USB2.0 HOST interface
		1-CH USB Type-c interface

	Camera Interface	2-CH MIPI-CSI (4-channel), support two camera inputs at the same time, resolution up to 2*1080p@80Hz
	Input Interface	Standard I2C capacitive screen interface
	Expansion Interface （Choose 1 of 2）	MINI-PCIE interface (USB2.0), to connect 4G external module
		M.2 B-KEY interface, to connect 5G external module, SIM card interface
	Expansion Interface	8-CH GPIO interface (1.8V)
	Storage Interface	1-CH TF card interface
		1-CH SATA interface
	Other Devices	Reset circuit, watchdog circuit, real-time clock
	Power input	+12V power supply
Provide information	Development Tools	Development environment: VM15.5.0 + Ubuntu20.04 or other Linux environment
		Debugging tools for application development use
		Cross-compiler
		Common terminal development and debugging tools
	System images	Image file of the corresponding operating system
	Test programs	Interface application demo test program and test program source code
	Source Code	Bootloader, kernel, file system source code
	Manuals	Hardware manuals, test manuals, device manuals, etc.
	Schematics	Schematic diagram of the base board (PDF file)
	Mechanical diagram	Base board structure dimensional drawing (DXF file)
Electrical Characteristics	Board layer/size	Core board size: 65mm*70mm, 8-layer board high-precision immersion gold process.
		Bottom board size: 200mm * 140mm, 4-layer board high-precision immersion gold process.
	Power Consumption	＜3W(Non-loaded)
	Operating Temperature	0℃ ~ +70℃(Industrial grade temperature width -40℃ ~ +85 ℃ can be selected according to customers' requirements)
	Storage Temperature	-0℃ ~ +70℃

	Operating Humidity	10% to 90%, non-condensing
	Core Board Option 1	Default configuration 2GB DDR/8GB eMMC
	Core Board Option 2	Optional configuration 4GB DDR/16GB eMMC

2.3 Core Board Resources

IAC-RK3568-CM core board adopts 8-layer PCB board with high-precision immersed gold process and high TG board, which has reliable electrical performance and anti-interference performance; integrated CPU, LPDDR4, eMMC, power management chip, etc.; up to 200 pins are introduced by board-to-board connector, which fully expands the hardware resources of RK3568 processor, and different interface functions can be combined according to the pin situation multiplexed to make a backplane that meets the requirements.

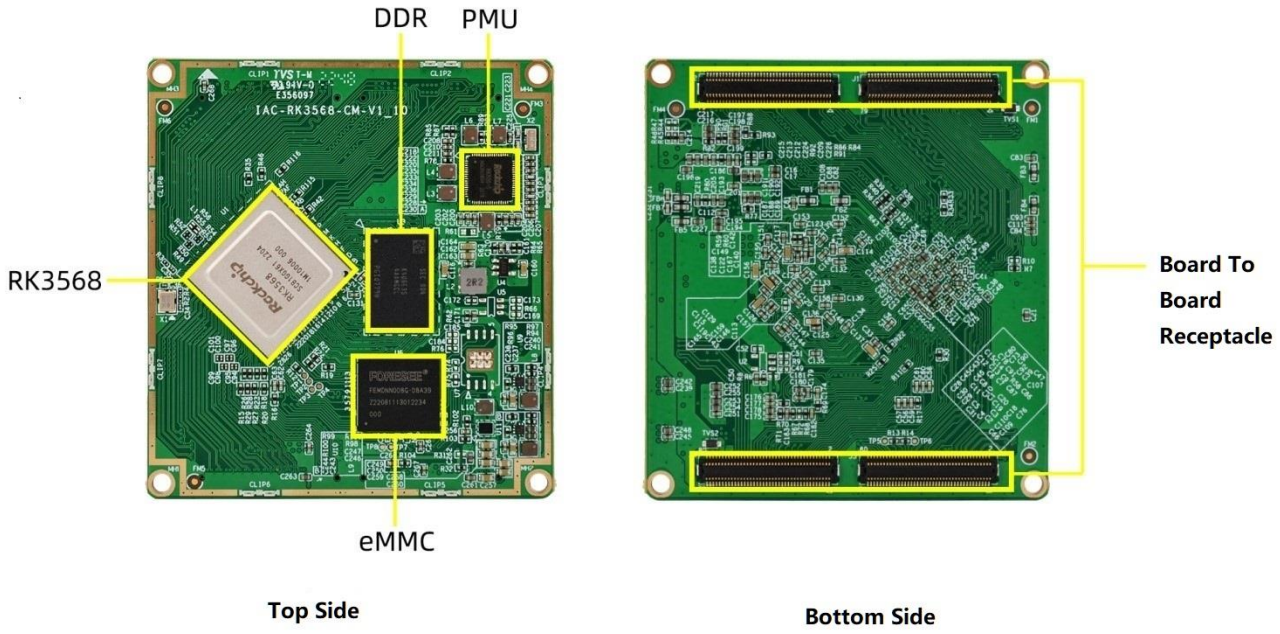

Chart 2

◆ On-board RockChip RK3568 processor.

◆Onboard 2GB LPDDR4, 8GB eMMC (default configuration).

◆The core board adopts 8-layer PCB board with high-precision immersion gold process.

◆Core board size: 65mm*70mm, suitable for various embedded occasions.

◆The core board adopts four 2*40Pin board-to-board connectors to lead the core board resources.

◆Using 5V power supply and on-board power management chip.

◆Support Debian 10.0 system.

◆Support Android 11.0 system.

Core board pinout resource interface pin definitions refer to the bottom board interface function section.

III. Baseboard Interface Function

Interface Block Diagram – Tope Side

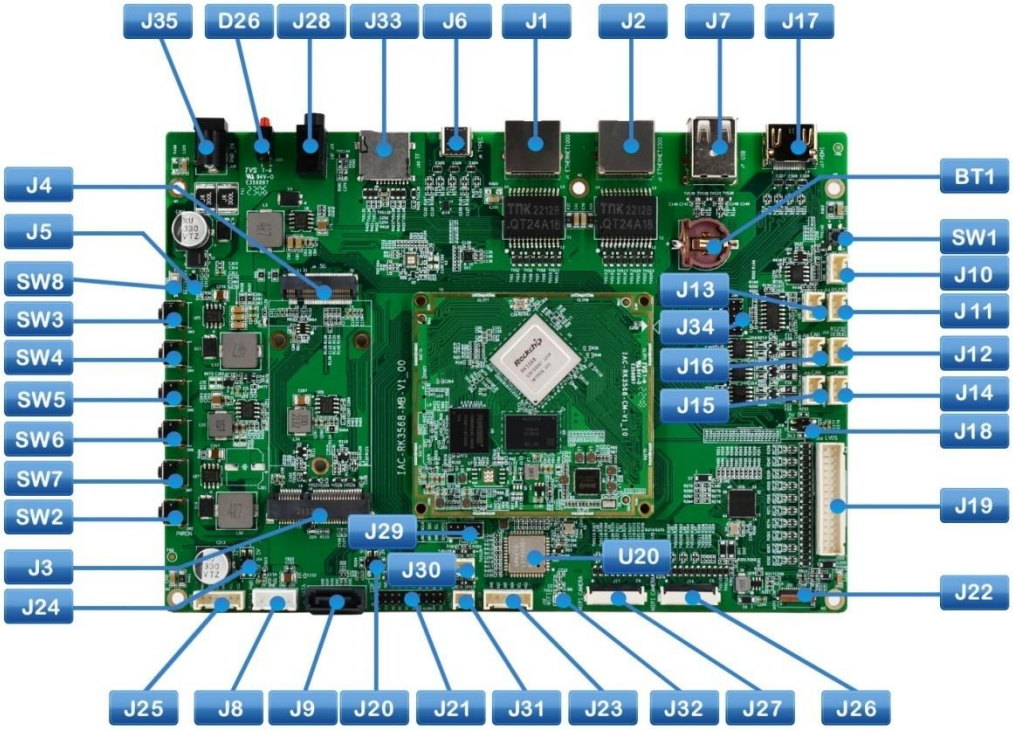

Chart 3

Interface Block Diagram – Bottom Side

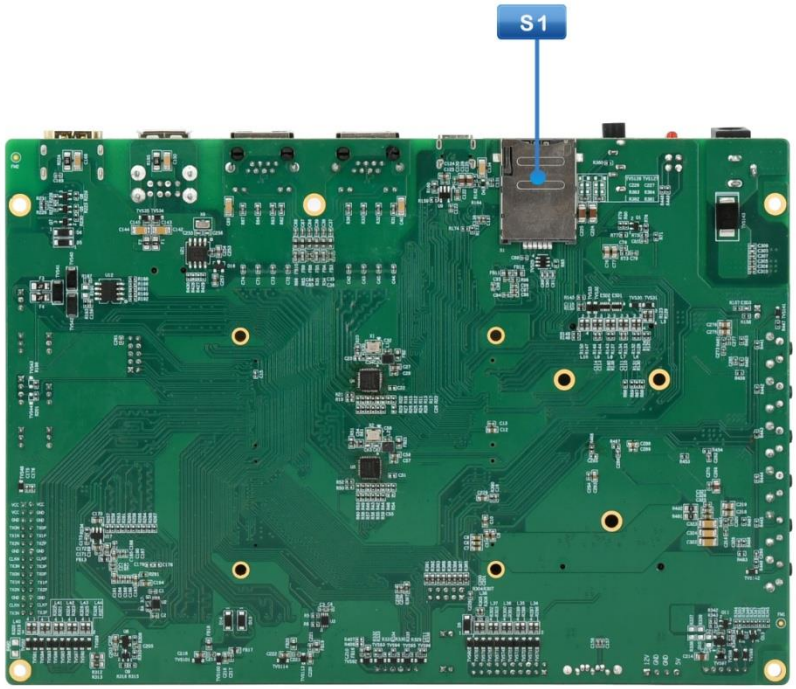

Chart 4

3.1 Description of basic interfaces functions

Label #	Function
J35	DC12V Power In
D26	Power indicator, system operation indicator
J28	Headphone socket (dual channel audio output)
J33	TF card slot
J6	Type-c Interface
J1	Gigabit Ethernet interface
J2	Gigabit Ethernet interface
J7	USB2.0 HOST Interface（2*USB2.0）
J17	HDMI Output Interface
BT1	RTC Battery
SW1	RESET Button
J10	RS485 Interface
J11	RS232 Interface
J12	UART Debug Port (TTL level)
J14	CAN Interface
J18	3.3V/5V Jumpers
J19	LVDS Interface
J13	RS232 Interface
J34	SPI、I2C Interface
J16	CAN Interface
J15	CAN Interface
J22	MIPI-DSI Interface
J26	MIPI-CSI Interface

J27	MIPI-CSI Interface
J32	WiFi-IPEX Antenna Socket
J23	I2C Interface（TP）
J31	Speak Output Interface
J21	EDP Interface
J20	3.3V/5V Jumpers
J9	SATA Interface
J8	SATA Power supply interface
J25	Backlight interface（12V/5V）
U20	WiFi Module
J29	I2S、I2C Interface
J30	MIC Input Interface
J24	12V/5V Jumpers
J3	MINI-PCIE Sockets
J4	M.2 B-KEY Sockets
J5	USB-OTG（HOST/Device）
S1	SIM card slot (back)
SW2	PMIC_PWRON Button
SW3-7	KEY Function button
SW8	Recovery Button

3.2 Interface Pin Definitions

J1A：（Core board interface’s pins definition）

Multiplexing GPIO	Signal Name	PIN#	PIN#	Signal Name	Multiplexing GPIO
	SYS_RESETn	1	2	GPIO_CC_nINT	GPIO0_A0_d
GPIO0_A4_u	SDMMC0_DET_L	3	4	GND	
GPIO0_A5_d	GPIO_WDT_FEED	5	6	GPIO_TYPEC_XSD	GPIO4_D2_d
GPIO0_A6_d	GPIO_WDT_EN	7	8	GPIO_TYPEC_SEL	GPIO4_C5_d
	VCC_PMU_3V3	9	10	GPIO_USB1_PWREN	GPIO4_C6_d
	GND	11	12	CAN1_TXD	GPIO4_C3_d
GPIO0_B6_u	SPI0_MOSI	13	14	CAN1_RXD	GPIO4_C2_d
GPIO0_B5_u	SPI0_CLK	15	16	GPIO_RUN_LED	GPIO4_C4_d
GPIO0_C5_d	SPI0_MISO	17	18	GND	
GPIO0_C6_d	SPI0_CS0	19	20	HDMI_TX_D2P	
GPIO0_B4_u	CAN0_RXD	21	22	HDMI_TX_D2N	
GPIO0_B3_u	CAN0_TXD	23	24	HDMI_TX_D1P	
GPIO0_B0_U	GPIO_BT_REG_ON	25	26	HDMI_TX_D1N	
GPIO0_C3_d	PWM4_OUT	27	28	HDMI_TX_D0P	
GPIO0_B7_d	PWM0_OUT	29	30	HDMI_TX_D0N	
GPIO0_C4_d	UART0_RTSn	31	32	HDMI_TX_CLKP	
GPIO0_C7_d	UART0_CTSn	33	34	HDMI_TX_CLKN	
GPIO0_C0_d	UART0_RXD	35	36	GND	
GPIO0_C1_d	UART0_TXD	37	38	HDMITX_SCL	GPIO4_C7_u
GPIO0_C2_d	EDP_HPDIN	39	40	HDMITX_SDA	GPIO4_D0_u
GPIO0_D1_u	UART2_RXD	41	42	HDMITX_CEC_M0	GPIO4_D1_u
GPIO0_D0_u	UART2_TXD	43	44	HDMI_TX_HPDIN	
	GND	45	46	GND	

	MIPI_DSI_TX1_D0N	47	48	MIPI_DSI_TX0_D0N/LVDS_TX0_D0N	
	MIPI_DSI_TX1_D0P	49	50	MIPI_DSI_TX0_D0P/LVDS_TX0_D0P	
	MIPI_DSI_TX1_D1N	51	52	MIPI_DSI_TX0_D1N/LVDS_TX0_D1N	
	MIPI_DSI_TX1_D1P	53	54	MIPI_DSI_TX0_D1P/LVDS_TX0_D1P	
	MIPI_DSI_TX1_CLKN	55	56	MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN	
	MIPI_DSI_TX1_CLKP	57	58	MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP	
	MIPI_DSI_TX1_D2N	59	60	MIPI_DSI_TX0_D2N/LVDS_TX0_D2N	
	MIPI_DSI_TX1_D2P	61	62	MIPI_DSI_TX0_D2P/LVDS_TX0_D2P	
	MIPI_DSI_TX1_D3N	63	64	MIPI_DSI_TX0_D3N/LVDS_TX0_D3N	
	MIPI_DSI_TX1_D3P	65	66	MIPI_DSI_TX0_D3P/LVDS_TX0_D3P	
	GND	67	68	GND	
	MIPI_CSI_RX_D2N	69	70	MIPI_CSI_RX_D0N	
	MIPI_CSI_RX_D2P	71	72	MIPI_CSI_RX_D0P	
	MIPI_CSI_RX_D3N	73	74	MIPI_CSI_RX_D1N	

	MIPI_CSI_RX_D3P	75	76	MIPI_CSI_RX_D1P	
	MIPI_CSI_RX_CLK1N	77	78	MIPI_CSI_RX_CLK 0N	
	MIPI_CSI_RX_CLK1P	79	80	MIPI_CSI_RX_CLK 0P	

J1B：（Core board interface's pin definition）

Multiplexing GPIO	Signal Name	PIN#	PIN#	Signal Name	Multiplexing GPIO
GPIO3_A1_d	GPIO_4G_PLUG_DET	1	2	GPIO_5G_PLUG_D ET	GPIO3_A0_d
GPIO3_A2_d	I2S3_MCLK	3	4	GND	
GPIO3_A3_d	I2S3_SCLK	5	6	PCIE30X2_CLKRE Qn	GPIO2_D4_d
GPIO3_A4_d	I2S3_LRCK	7	8	PCIE30X2_WAKEn	GPIO2_D5_d
GPIO3_A5_d	I2S3_SDO	9	10	PCIE30X2_PERSTn	GPIO2_D6_d
GPIO3_A6_d	I2S3_SDI	11	12	GPIO_5G_ON_OFF	GPIO2_D7_d
GPIO3_A7_d	GPIO_REV1	13	14	GPIO_MDL_DISEN	GPIO2_D0_d
	GND	15	16	GPIO_MDL_nRST	GPIO2_D1_d
GPIO3_B0_d	GPIO_CLK_nCLKRE Q	17	18	GPIO_MDL_PWR_ CFG	GPIO2_D2_d
	GND	19	20	GPIO_MDL_PWR_E N	GPIO2_D3_d
GPIO3_B2_d	UART4_TXD	21	22	GND	
GPIO3_B1_d	UART4_RXD	23	24	I2C3_SDA	GPIO3_B6_d
GPIO3_C3_d	UART5_RXD	25	26	I2C3_SCLCL_M1	GPIO3_B5_d
GPIO3_C2_d	UART5_TXD	27	28	I2C5_SCL	GPIO3_B3_d

GPIO3_C1_d	GPIO_RS485_DIR	29	30	I2C5_SDA	GPIO3_B4_d
GPIO3_C4_d	UART7_TXD	31	32	GPIO_TP_nRST	GPIO3_B7_d
GPIO3_C5_d	UART7_RXD	33	34	GPIO_TP_nINT	GPIO3_C0_d
	GND	35	36	GND	
GPIO3_D0_d	SDMMC2_D2	37	38	SDMMC2_CLK	GPIO3_D3_d
GPIO3_C6_d	SDMMC2_D0	39	40	SDMMC2_D3	GPIO3_D1_d
GPIO3_C7_d	SDMMC2_D1	41	42	SDMMC2_CMD	GPIO3_D2_d
GPIO3_D4_d	GPIO_WIFI_REG_ON	43	44	GPIO_GMAC1_nRST	GPIO3_D5_d
	GND	45	46	GND	
GPIO4_A0_d	GMAC1_TXCLK	47	48	GMAC1_RXCLK	GPIO4_A3_d
GPIO4_A4_d	GMAC1_TXD0	49	50	GMAC1_RXD2	GPIO4_A1_d
GPIO4_A5_d	GMAC1_TXD1	51	52	GMAC1_RXD3	GPIO4_A2_d
GPIO3_D7_d	GMAC1_TXD3	53	54	GMAC1_RXD0	GPIO4_A7_d
GPIO3_D6_d	GMAC1_TXD2	55	56	GMAC1_RXDV_CRS	GPIO4_B1_d
GPIO4_A6_d	GMAC1_TXEN	57	58	GMAC1_RXD1	GPIO4_B0_d
	GND	59	60	GND	
GPIO4_B7_d	GMAC1_MDIO	61	62	GMAC1_MCLKINOUT_M1/CIF_CLKIN	GPIO4_C1_d
GPIO4_B6_d	GMAC1_MDC	63	64	GND	
	GND	65	66	I2C4_SCL	GPIO4_B3_d
GPIO4_C0_d	GPIO_GMAC1_nINT	67	68	I2C4_SDA	GPIO4_B2_d
	GND	69	70	GND	
GPIO4_B4_d	CAN2_RXD	71	72	USB2_HOST3_DP	
GPIO4_B5_d	CAN2_TXD	73	74	USB2_HOST3_DM	

	GND	75	76	GND	
GPIO0_B2	I2C0_SDA	77	78	USB2_HOST2_DP	
GPIO0_B1	I2C0_SCL	79	80	USB2_HOST2_DM	

J1C：（Core Board interface’s pin definition）

Multiplexing GPIO	Signal Name	PIN#	PIN3	Signal Name	Multiplexing GPIO
	SATA2_RXN	1	2		
	SATA2_RXN	3	4		
	GND	5	6	PCIE30_RX0N	
	SATA2_TXN	7	8	PCIE30_RX0P	
	SATA2_TXP	9	10	GND	
	GND	11	12		
		13	14		
		15	16	PCIE30_TX0N	
	GND	17	18	PCIE30_TX0P	
	USB3_HOST1_SSTXP	19	20	GND	
	USB3_HOST1_SSTXN	21	22	PCIE30_REFCLKP_IN	
	GND	23	24	PCIE30_REFCLKN_IN	
	USB3_HOST1_SSRXP	25	26	GND	
	USB3_HOST1_SSRXN	27	28	USB3_OTG0_DM	
	GND	29	30	USB3_OTG0_DP	
	USB3_OTG0_SSTXP	31	32	USB3_OTG0_ID	
	USB3_OTG0_SSTXN	33	34	USB3_OTG0_VBUS	

				DET	
	GND	35	36	GND	
	USB3_OTG0_SSRXP	37	38	MULTI_PHY1_REF CLKN	
	USB3_OTG0_SSRXN	39	40	MULTI_PHY1_REF CLKP	
	GND	41	42	MULTI_PHY0_REF CLKN	
	EDP_TX_D3N	43	44	MULTI_PHY0_REF CLKP	
	EDP_TX_D3P	45	46	GND	
	EDP_TX_D2N	47	48	USB3_HOST1_DM	
	EDP_TX_D2P	49	50	USB3_HOST1_DP	
	EDP_TX_D1N	51	52	GND	
	EDP_TX_D1P	53	54	SDMMC0_CLK	GPIO2_A2_d
	EDP_TX_D0N	55	56	SDMMC0_D3	GPIO2_A0_u
	EDP_TX_D0P	57	58	SDMMC0_D1	GPIO1_D6_u
	EDP_TX_AUXP	59	60	SDMMC0_D0	GPIO1_D5_u
	EDP_TX_AUXN	61	62	SDMMC0_D2	GPIO1_D7_u
	GND	63	64	SDMMC0_CMD	GPIO2_A1_u
	VCC_SD_3V3	65	66	VCC_IO_SD	
	GND	67	68	GND	
GPIO2_B5_u	GMAC0_TXEN	69	70	GMAC0_RXD2	GPIO2_A3_u
GPIO2_B4_u	GMAC0_TXD1	71	72	GMAC0_RXD3	GPIO2_A4_u
GPIO2_B3_u	GMAC0_TXD0	73	74	GMAC0_RXD0	GPIO2_B6_u
GPIO2_B0_d	GMAC0_TXCLK	75	76	GMAC0_RXDV_CR	GPIO2_C0_d

				S	
GPIO2_A7_u	GMAC0_TXD3	77	78	GMAC0_RXD1	GPIO2_B7_d
GPIO2_A6_u	GMAC0_TXD2	79	80	GMAC0_RXCLK	GPIO2_A5_u

J1D：（Core board interface's pin definition）

Multiplexing GPIO	Signal Name	PIN#	PIN3	Signal Name	Multiplexing GPIO
GPIO2_C5_d	GPIO_GMAC0_nRST	1	2	GMAC0_MDC	GPIO2_C3_d
GPIO2_C6_d	GPIO_GMAC0_nINT	3	4	GMAC0_MDIO	GPIO2_C4_d
GPIO2_B2_u	GPIO_LCD_MIPI_nRST	5	6	GND	
GPIO2_B1_d	GPIO_BL0_EN	7	8	GMAC0_MCLKINOUT	GPIO2_C2_d
	GND	9	10	GND	
GPIO0_D3_d	GPIO_BL0_PWR_EN	11	12	ETH0_REFCLKO_25M	GPIO2_C1_d
GPIO0_D5_D	GPIO_BL1_PWR_EN	13	14	GND	
GPIO0_D6_D	GPIO_LT9211_nINT	15	16		
GPIO0_D4_d	GPIO_LT9211_nRST	17	18		
	VCC_PMU_1V8	19	20	RECOVERY	
	GND	21	22		
GPIO1_B0_d	GPIO_CAM_MIPI_PWDN	23	24		
GPIO1_B1_d	GPIO_CAM_MIPI_nRST	25	26		
GPIO1_A4_d	GPIO_CAM0_PWR_EN	27	28		

GPIO1_B2_d	GPIO_CAM1_PWR_EN	29	30		
	GND	31	32	GND	
GPIO1_A1_u	GPIO_WIFI_nINT	33	34	VCC_ADC_1V8	
GPIO1_A0_u	GPIO_BT_nINT	35	36	GND	
	GND	37	38		GPIO1_D4_u
	VCC_IO_CODEC	39	40		GPIO1_D1_u
	GND	41	42		GPIO1_D2_u
	PMIC_HPL_OUT	43	44		GPIO1_D3_u
	PMIC_HPL_SNS	45	46		
	PMIC_HPR_OUT	47	48	GND	
	GND	49	50		GPIO1_D0_d
	PMIC_SPKOUT_N	51	52	GND	
	PMIC_SPKOUT_P	53	54		
	GND	55	56	PMIC_PWRON	
	PMIC_MIC1_N	57	58	GND	
	PMIC_MIC1_P	59	60	PMIC_CLK32K_OUT	
	GND	61	62	GND	
	VCC_IO_3V3	63	64	VCC_IO_1V8	
	VCC_IO_3V3	65	66	VCC_IO_1V8	
	GND	67	68	GND	
	GND	69	70	GND	
	GND	71	72	GND	
	GND	73	74	GND	
	VCC_SYS_5V0	75	76	VCC_SYS_5V0	

	VCC_SYS_5V0	77	78	VCC_SYS_5V0	
	VCC_SYS_5V0	79	80	VCC_SYS_5V0	

J10：RS485 Interface

Pin No.	Signal Name
1	RS485_B
2	RS485_A
3	GND

J11/J13：RS232 Interface

Pin No.	Signal Name
1	TXD
2	RXD
3	GND

J12： UART Debug port

Pin No.	Signal Name
1	TXD
2	RXD
3	GND

J14/J15/J16：CAN Interface

Pin No.	Signal Name
1	CAN_H
2	CAN_L
3	GND

J18：3.3V/5.0V Jumper Interface

Signal Name	PIN#	PIN#	Signal Name
VCC_LVDS_LCD	1	2	VCC_EXT_5V0
VCC_LVDS_LCD	3	4	VCC_EXT_3V3

J19：LVDS Interface

Signal Name	PIN#	PIN#	Signal Name
VCC_LVDS_LCD	1	2	VCC_LVDS_LCD
VCC_LVDS_LCD	3	4	GND
GND	5	6	GND
LCD_LVDSA_TX0_N	7	8	LCD_LVDSA_TX0_P
LCD_LVDSA_TX1_N	9	10	LCD_LVDSA_TX1_P
LCD_LVDSA_TX2_N	11	12	LCD_LVDSA_TX2_P
GND	13	14	GND
LCD_LVDSA_CLK_N	15	16	LCD_LVDSA_CLK_P
LCD_LVDSA_TX3_N	17	18	LCD_LVDSA_TX3_P
LCD_LVDSB_TX0_N	19	20	LCD_LVDSB_TX0_P
LCD_LVDSB_TX1_N	21	22	LCD_LVDSB_TX1_P
LCD_LVDSB_TX2_N	23	24	LCD_LVDSB_TX2_P
GND	25	26	GND
LCD_LVDSB_CLK_N	27	28	LCD_LVDSB_CLK_P
LCD_LVDSB_TX3_N	29	30	LCD_LVDSB_TX3_P

J22：MIPI-DSI Interface

Pin No.	Signal Name

1	VCC_LED+
2	VCC_LED+
3	VCC_LED+
4	NC
5	VCC_LED-
6	VCC_LED-
7	VCC_LED-
8	VCC_LED-
9	GND
10	GND
11	LCD_MIPI_D2_P
12	LCD_MIPI_D2_N
13	GND
14	LCD_MIPI_D1_P
15	LCD_MIPI_D1_N
16	GND
17	LCD_MIPI_CLK_P
18	LCD_MIPI_CLK_N
19	GND
20	LCD_MIPI_D0_P
21	LCD_MIPI_D0_N
22	GND
23	LCD_MIPI_D3_P
24	LCD_MIPI_D3_N
25	GND

26	NC
27	LCD_MIPI_nRST
28	NC
29	VCC_EXT_1V8
30	VCC_EXT_3V3
31	VCC_EXT_3V3

J26： MIPI-DSI Interface

Pin No.	Signal Name
1	VCC_EXT_5V0
2	GND
3	VCC_EXT_3V3
4	VCC_EXT_3V3
5	GND
6	CAM_MIPI_CLK0_N
7	CAM_MIPI_CLK0_P
8	GND
9	CAM_MIPI_D0_N
10	CAM_MIPI_D0_P
11	GND
12	CAM_MIPI_D1_N
13	CAM_MIPI_D1_P
14	GND
15	NC
16	NC

17	GND
18	NC
19	NC
20	GND
21	CAM0_MIPI_I2C_SDA
22	CAM0_MIPI_I2C_SCL
23	CAM0_MIPI_PWDN
24	CAM0_MIPI_nRST
25	GND
26	CAM0_MIPI_PWR_EN

J27： MIPI-CSI Interface

Pin No.	Signal Name
1	VCC_EXT_5V0
2	GND
3	VCC_EXT_3V3
4	VCC_EXT_3V3
5	GND
6	CAM_MIPI_CLK1_N
7	CAM_MIPI_CLK1_P
8	GND
9	CAM_MIPI_D2_N
10	CAM_MIPI_D2_P
11	GND
12	CAM_MIPI_D3_N

13	CAM_MIPI_D3_P
14	GND
15	NC
16	NC
17	GND
18	NC
19	NC
20	GND
21	CAM1_MIPI_I2C_SDA
22	CAM1_MIPI_I2C_SCL
23	CAM1_MIPI_PWDN
24	CAM1_MIPI_nRST
25	GND
26	CAM1_MIPI_PWR_EN

J23：I2C Interface（TP）

Pin No.	Signal Name
1	VCC_TP_3V3
2	TP_I2C_SCL
3	TP_I2C_SDA
4	TP_nINT
5	TP_nRST
6	GND

J31：Speak Output Interface

Pin No.	Signal Name

1	PMIC_SPKOUT_P
2	PMIC_SPKOUT_N

J21：EDP Interface

Signal Name	PIN#	PIN#	Signal Name
VCC_EDP_LCD	1	2	VCC_EDP_LCD
GND	3	4	GND
LCD_EDP_TX0_N	5	6	LCD_EDP_TX0_P
LCD_EDP_TX1_N	7	8	LCD_EDP_TX1_P
LCD_EDP_TX2_N	9	10	LCD_EDP_TX2_P
LCD_EDP_TX3_N	11	12	LCD_EDP_TX3_P
GND	13	14	GND
LCD_EDP_AUX_N	15	16	LCD_EDP_AUX_P
GND	17	18	GND
GND	19	20	LCD_EDP_HPD

J9：SATA Interface

Pin No.	Signal Name
1	GND
2	SATA2_TXP
3	SATA2_TXN
4	GND
5	SATA2_RXP
6	SATA2_RXN
7	GND

J8：SATA Power supply interface

Pin No.	Signal Name
1	VCC_EXT_12V0
2	GND
3	GND
4	VCC_EXT_5V0

J25：Backlight interface（12V/5V）

Pin No.	Signal Name
1	VCC_BL
2	VCC_BL
3	GND
4	GND
5	BL_EN
6	BL_PWM

J29：I2S、I2C Interface

Pin No.	Signal Name
1	VCC_EXT_3V3
2	I2S3_MCLK
3	I2S3_LRCK
4	I2S3_SCLK
5	I2S3_SDI
6	I2S3_SDO
7	GND
8	I2C3_SCL

9	I2C3_SDA
10	GPIO_REV1

J30：MIC Input Interface

Pin No.	Signal Name
1	PMIC_MIC1_P
2	PMIC_MIC1_N

J3：MINI-PCIE Socket

Signal Name	PIN#	PIN#	Signal Name
NC	1	2	VCC_4G_3V3
NC	3	4	GND
NC	5	6	NC
NC	7	8	4G_UIM_PWR
GND	9	10	4G_UIM_DATA
NC	11	12	4G_UIM_CLK
NC	13	14	4G_UIM_nRST
GND	15	16	NC
NC	17	18	GND
NC	19	20	4G_nDISEN
GND	21	22	4G_nRST
NC	23	24	VCC_4G_3V3
NC	25	26	GND
GND	27	28	NC
GND	29	30	NC
NC	31	32	NC

NC	33	34	GND
GND	35	36	4G_USB_D_N
GND	37	38	4G_USB_D_P
VCC_4G_3V3	39	40	GND
VCC_4G_3V3	41	42	4G_STATE
GND	43	44	NC
NC	45	46	NC
NC	47	48	NC
NC	49	50	GND
NC	51	52	VCC_4G_3V3

J4：M.2 B-KEY Socket

Signal Name	PIN#	PIN#	Signal Name
GND	1	2	VCC_5G_3V8
GND	3	4	VCC_5G_3V8
GND	5	6	5G_ON_OFF
5G_USB_D_P	7	8	5G_DISEN
5G_USB_D_N	9	10	5G_STATE
GND	11	…	STD B-KEY
STD B-KEY	…	20	NC
GND	21	22	NC
NC	23	24	NC
NC	25	26	NC
GND	27	28	NC
5G_USB_SSRX_N	29	30	5G_UIM_nRST

5G_USB_SSRX_P	31	32	5G_UIM_CLK
GND	33	34	5G_UIM_DATA
5G_USB_SSTX_N	35	36	5G_UIM_PWR
5G_USB_SSTX_P	37	38	1:USB3.0;0:PCIe
GND	39	40	NC
5G_PCIE_RX_N	41	42	NC
5G_PCIE_RX_P	43	44	NC
GND	45	46	NC
5G_PCIE_TX_N	47	48	NC
5G_PCIE_TX_P	49	50	5G_PCIE_nPERST
GND	51	52	5G_PCIE_nCLKREQ
5G_PCIE_REFCLK_N	53	54	5G_PCIE_nPEWAKE
5G_PCIE_REFCLK_P	55	56	NC
GND	57	58	NC
NC	59	60	NC
NC	61	62	NC
NC	63	64	NC
NC	65	66	NC
5G_nRST	67	68	NC
GND	69	70	VCC_5G_3V8
GND	71	72	VCC_5G_3V8
GND	73	74	VCC_5G_3V8
NC	75		

J5：USB-OTG（HOST/Device）

Pin No.	Signal Name
1	USB3_OTG0_ID
2	VCC_PMU_1V8

S1：SIM card slot (back)

Pin No.	Signal Name
1	VCC_SIM
2	SIM_nRST
3	SIM_CLK
4	GND
5	NC
6	SIM_DATA

IV. Structure & Size

Unit: mm, for connector size, please send email to: supports@qiyangtech.com；

4.1 Core Board Dimension

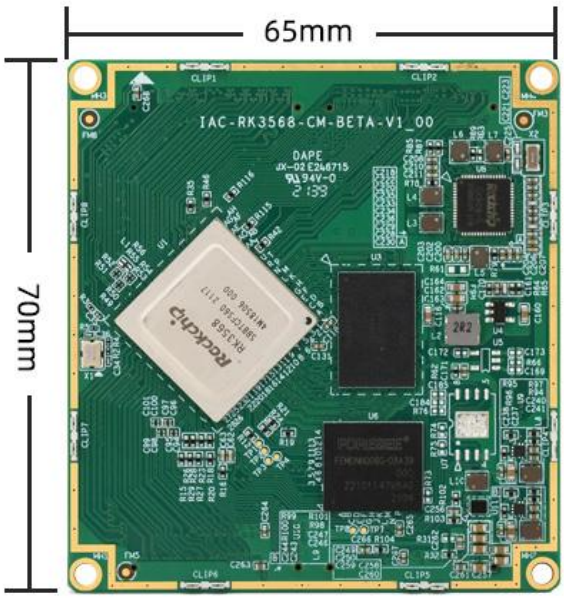

Chart 5

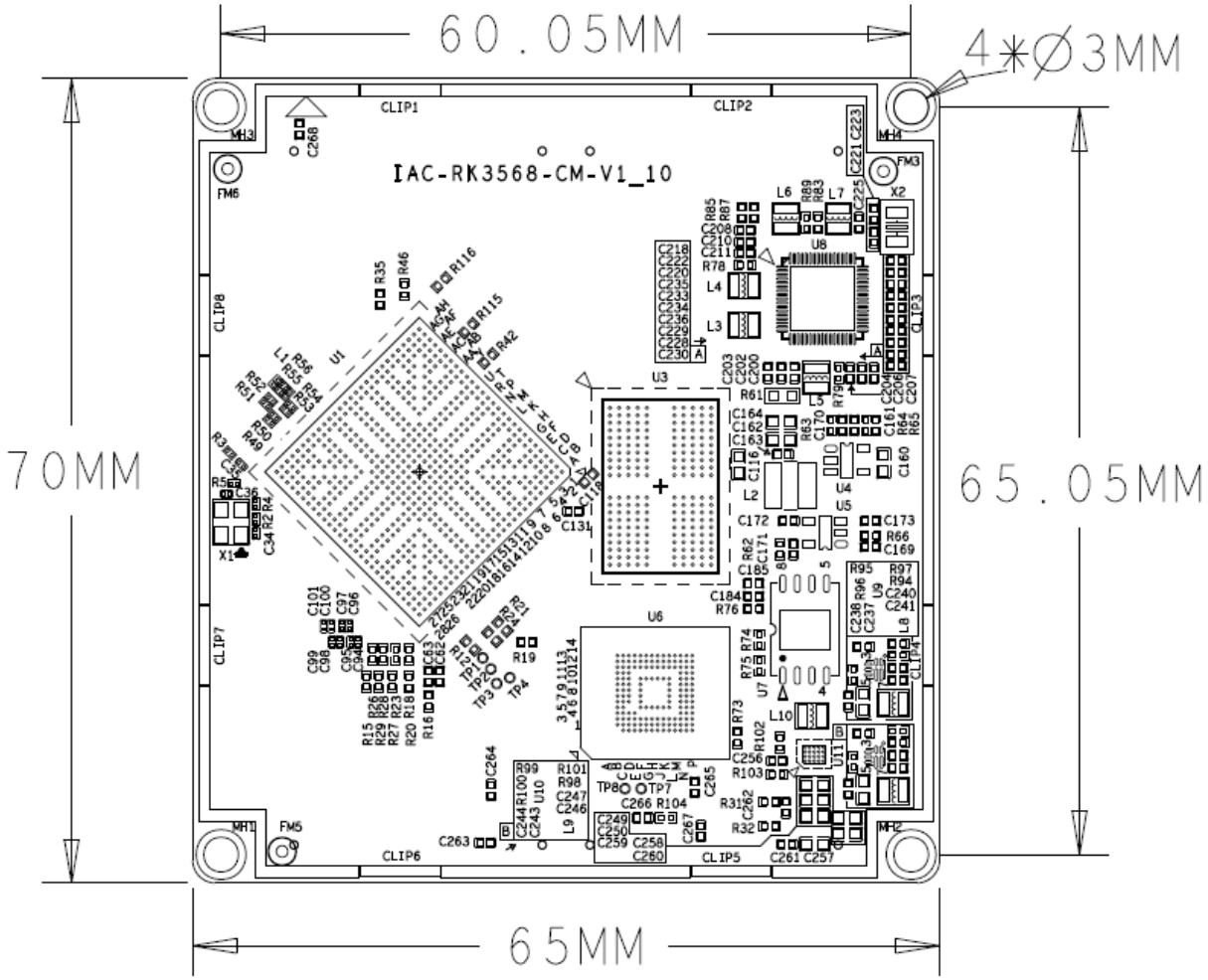

Chart 6

4.2 Base Board Dimension

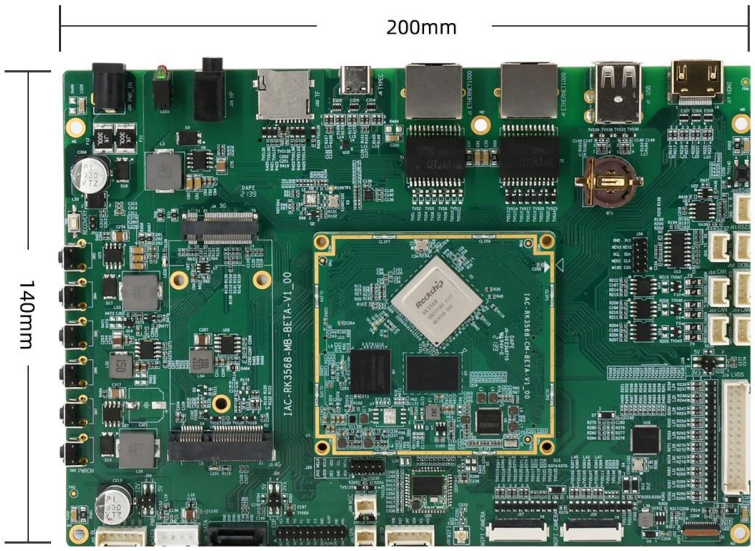

Chart 7

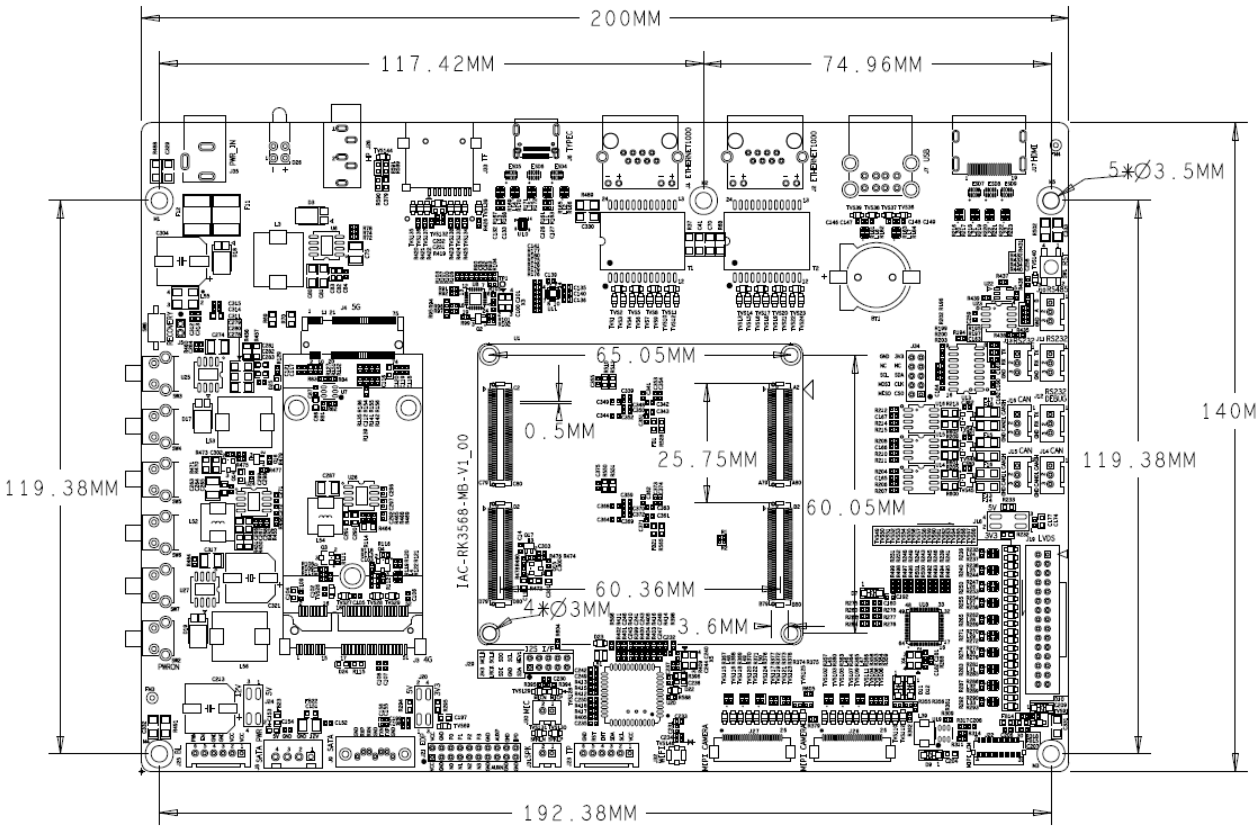

Chart 8

V. Connection Picture

Take a notice about the location of the Core Board

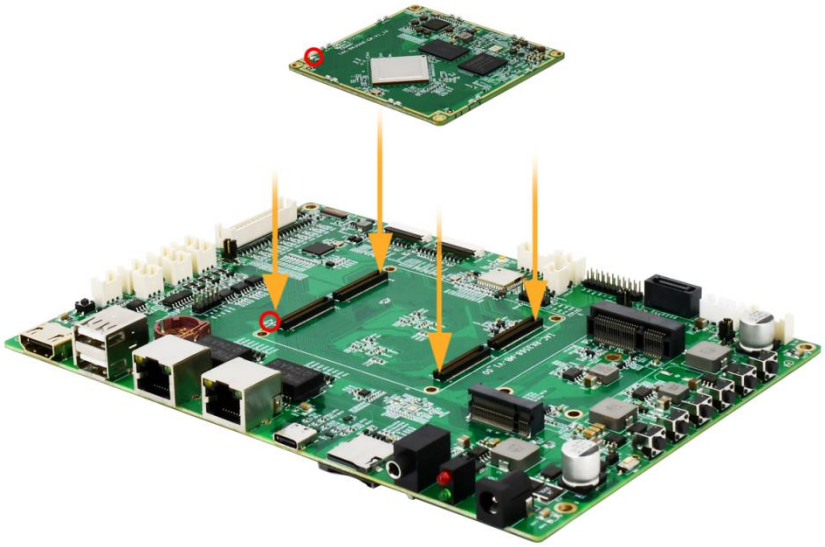

Chart 9

VI. Electrical Property

Items	Parameters
Operating temperature	0℃ ~ +70℃ (Industrial grade temperature :-40℃ ~ +85℃ is optional)
Storage Temperature	-10℃ ~ +70℃
Operating Humidity	10% ~ 95%, non-condensing
Core Board Size	66mm*70mm, 8-layer board high-precision gold-sinking process
Base Board Size	200mm*140mm, 4-layer board with high-precision gold plating process
Power consumption of the whole board	<3W (Non-loaded)
Power Supply	DC12V/2.5A

VII. Software Description

The software support provided by the IAC-RK3568-KIT mainly includes Linux /Android.

The IAC-RK3568-KIT Linux User's Manual describes in detail the establishment and use of the Linux development environment provided by the IAC-RK3568-KIT development board, please refer to the related documentation for more details.

The IAC-RK3568-KIT Android User's Manual describes in detail the establishment and use of the Android development environment provided by the IAC-RK3568-KIT development board, for more details, please refer to the related documentation.

VIII. Note

1.

- Exceeding the warranty service period.
- No valid purchase documents.
- Into the liquid, moisture or mold.
- Failure and damage caused by non-quality reasons such as dropping, strong vibration or unauthorized alteration or misuse after purchase.
- Damage caused by force majeure.

2. Our company retains the intellectual property rights of all IAC-RK3568-KIT products with independently developed related software and hardware technical data; users can only use them for teaching, experimental and scientific research purposes, and cannot engage in any commercial use, nor can they distribute them on the network, or tamper with their copyrights by interception or modification.

3. This product accepts customers' bulk order, and the company will provide full technical support and service.

Zhejiang Qiyang Intelligent Technology Co.,Ltd

Tel：0571-87858811 / 87858822

Fax：0571-89935912

Technology Support：0571-87858811 ext. 805

E-MAIL：supports@qiyangtech.com

Website： http://www.qiytech.com

Address：3F, Building A, No.6 West Park 8th Road, West Lake Science and Technology Park, West Lake District, Hangzhou, China

Post code：310030